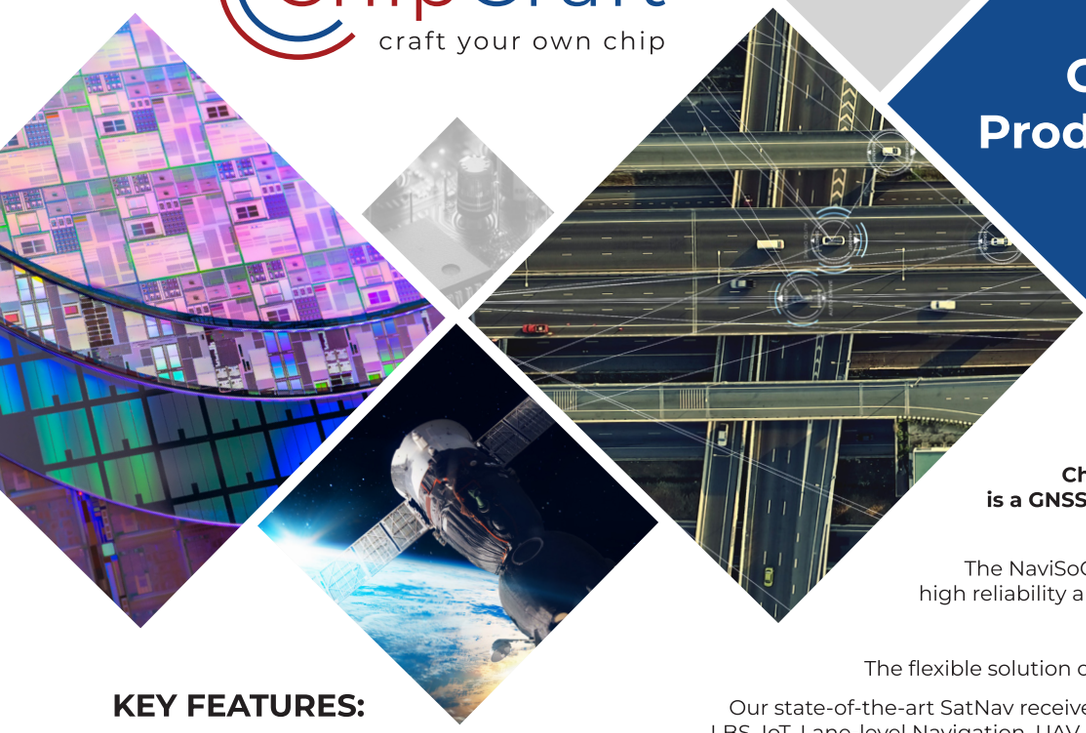
ChipCraft®
craft your own chip



GNSS Products

NAVISOC IC

ChipCraft's flagship product, the NaviSoC, is a GNSS receiver integrated with an application processor, on a single silicon die.

The NaviSoC system on a chip delivers high precision, high reliability and security, with low power consumption, in a small size.

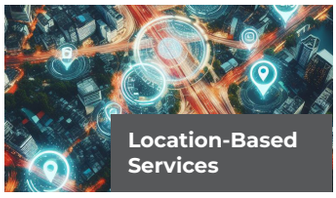
The flexible solution offers customization to user requirements.

Our state-of-the-art SatNav receiver serves variety of applications, including LBS, IoT, Lane-level Navigation, UAV and Autonomous Drones, Asset Tracking, Time Synchronization, Smart Agriculture, Surveying and Mapping.

KEY FEATURES:

- Multi-Frequency and Multi-Constellation
- Global Coverage
- Fast TTFF
- Centimeter-Level Accuracy
- Dead Reckoning
- RTK
- High Sensitivity
- High Update Rate
- Flexible Supply Voltage
- Low Power Consumption
- RISC-V Application MCU
- Variety of Peripherals and Interfaces
- Embedded Flash
- Dedicated SDK and IDE

APPLICATIONS:


Location-Based Services


IoT


Micromobility

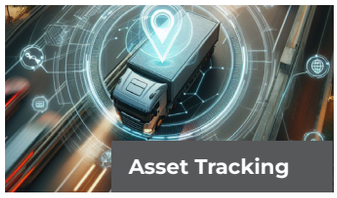

Automotive Navigation


Railway Navigation


Lane-Level Navigation


UAV and Autonomous Drones


Autonomous Vehicles

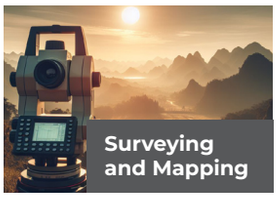

Asset Tracking


Time Synchronization


Industrial Machinery Navigation and Tracking


Smart Agriculture


Infrastructure and Buildings Monitoring


Surveying and Mapping

Reach out to us:

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TECHNICAL DATA

GNSS hardware resources	
GNSS Constellations and Frequencies:	
GPS:	L1C/A, L1C, L2C, L5
Galileo:	E1B, E5a, E5b, E6B
GLONASS (FDMA):	L1OF, L2OF
GLONASS (CDMA):	L1OC, L2OC, L3OC
Beidou (Phase 2):	B1I, B3I (MEO, GEO, GSYNC)
Beidou (Phase 3):	B1C, B2a
QZSS:	L1C/A, L1C, L2C, L5
IRNSS:	NavIC L5
SBAS:	EGNOS, WAAS, GAGAN, MSAS, SDCM
Number of Tracking Channels:	
192 hardware channels for simultaneous tracking	
Other features:	
· Dedicated acquisition engine · Able to acquire and track all in view satellites of all systems and frequencies as specified above	

GNSS performance data	
Accuracy:	
PVT <1 m CEP **HAS** 0.2 m horizontal, 0.4 m vertical **RTK** 0.01 m horizontal, 0.03 m vertical	
Time To First Fix	
tested with simulator, nominal signal power -160 dBW, TTFF > 50%	
Cold start (no almanac, no approx. position):	26s
Warm start (no ephemeris, approx. position known):	24s
Hot start (re-acquisition with valid time, position, almanac and ephemeris data):	1s
Sensitivity	
to be tested with simulator, with external LNA, all satellites at same signal level allowed for re-acquisition	
Cold start:	-178 dbW
Hot start:	-187 dbW
Re-aquisition:	-190 dbW
Tracking:	-197 dbW
Navigation:	-195 dbW
Maximum update rate:	
Position (PVT):	10 Hz
Measurements only (RAW):	50 Hz
Accuracy of time pulse signal	
RMS	30 ns
99%	60 ns
Operational limits:	
Velocity:	500 m/s
Acceleration:	±40 m/s2
Altitude:	50 km
Other:	
· OSNMA · I/NAV improvements (RedCED, FEC2, SSP)	

Electrical, environmental and physical data	
Temperature Range:	-40°C ÷ 125°C
Power Supply:	1.62 ÷ 3.63 V
Backup Supply:	1.62 ÷ 3.63 V
Current Consumption (high performance mode):	< 100 mA @ 3.0 V
Current Consumption (low power mode):	tailored to application
Package:	
Type: QFN and WLCSP Size: 10 x 10 x 0.8 mm (QFN); 5.8 x 6.2 x 0.3 mm (WLCSP)	
Interfaces:	
· 4x UART · 3x SPI Master/Slave) · 2x I2C (Master/Slave) · HyperBus · 2x CAN · 1-Wire · Configurable PPS out · Configurable PPS in (external high stability clock) · 32x GPIO user programmable · JTAG debugging capability	
Protocols:	
· NMEA 3.01, 4.11 · RTCM v3.3 · AT commands	
Timers:	
· One Real-Time Counter (RTC) (32 bits, 32.768 kHz) · Two general-purpose 32-bit timers · Two general-purpose 16-bit timers · One 24-bit system tick timer · One 56-bit counter for timestamps · Watchdog timer	
Multicore RISC-V based 32-bit CPU::	
· Double-precision Floating Point Unit (FPU) · Physical Memory Protection Unit (PMP) · 2 MB internal SRAM · 2 MB eFlash NVM (AEC-Q100 grade 2) · Operating frequency up to 280 MHz	
RF data:	
· LNA: Built-In (no external LNA required) · Overall noise figure 2.5 dB (internal LNA + RF + IF + ADC combined)	
Other	
· Power management unit, with separate power supply domain and on-chip DC/DC and LDO · Separate RF domain with dedicated LDO · IO-ring 1.8/2.5/3.3 V capable with on-chip LDO · Fail safe GPIOs · ESD: 2 kV (HBM) and 500 V (CDM)	

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