Warsaw, 18.01.2021

REQUEST FOR OFFER No 03/2020

concerning the procedure conducted on the basis of the principles of fair competition and equal treatment of contractors, transparency, economy, impartiality and objectivity for public contracts with a value higher than or equal to PLN 120,000, in accordance with the regulations of the competition carried out as part of the Path for Mazovia competition announced by the National Research Center and Development

1. Ordering Party

ChipCraft Sp. z o.o.
ul. Bohdana Dobrzańskiego 3 lok. BS073
20-262 Lublin
NIP 9462659910
REGON 364311086

2. Description of the subject of the inquiry

A) The subject of the contract is a service consisting in the supply of commercial EDA / CAD software licenses for the design of integrated circuits necessary for the implementation of the project under the name: "Navigation microcontroller for centimeter satellite navigation with hardware position authentication for autonomous devices".

B) A more detailed description of the subject of the inquiry is attached as Attachment No 2.

C) The Ordering Party does not allow partial and variant offers.

D) The Ordering Party does not provide for the possibility of awarding supplementary contracts.

E) Offer validity: minimum 5 days.

F) The Ordering Party is not obliged to conduct the procedure pursuant to the Act on Public Procurement.

3. Order completion date

Planned period of service implementation: no longer than 30 days from the date of order acceptance.

Projekt współfinansowany przez Narodowe Centrum Badań i Rozwoju w ramach programu Ścieżka dla Mazowsza
Umowa o dofinansowanie nr MAZOWSZE/0013/19-00

Digitally signed by Tomasz Borejko
Date: 2021.01.18 09:00:53 CET

4. Conditions for participation in the procedure and description of the method of evaluating their fulfillment

A) Offerer's eligibility

Only offerers who are in an economic and financial situation ensuring proper performance of the subject of the contract may participate in the procedure.

Offerers are excluded from the procedure:

- for which liquidation has been opened or bankruptcy has been announced
- who submitted untrue information that influences or may have an impact on the outcome of the proceedings
- related to the Employer
- submitted an incomplete, partial or variant offer

The offer of the excluded offerer is considered rejected.

B) Completeness of the offer

The offer should consist of the following documents and attachments signed by the offerer:

- Appendix No 1 - Offer form prepared in accordance with the template attached to the inquiry
- Appendix No 2 - Power of attorney of the authorized person signing the Offer *(if applicable)*

Guidelines for submitting documents:

The completed and signed Form of Offer should be submitted in accordance with the applicable templates attached to this Request for Offer. The documents in this procedure must be signed by the person(s) authorized to sign the offer. It is allowed to submit an offer in Polish and / or in English. The contracting authority will reject the offer if its content does not correspond to the content of this Request for Offer.

The assessment of compliance with the conditions for participation in the procedure will be made on the basis of the documents submitted by the Offerer in this procedure using the boundary condition method: meets - does not meet, and the basis for the assessment of compliance with the conditions will be the offerer's eligibility and the completeness of the offer.

C) Criteria and method of evaluation of offers

When selecting the offer, the Ordering Party will follow the principle of fair competition and equal treatment of contractors, transparency, economy, impartiality and objectivity.

The price in the offer must include all costs and components related to the performance of

the contract and the conditions set by the Ordering Party. Price variants are not allowed.

When selecting an offer, the Ordering Party will apply the following criteria: Price - 100%

Price (C)

The offerer who offers the lowest net price will receive the maximum number of points - 100. For the remaining offerers, the price scoring will be calculated according to the following formula:

C = (lowest offered net price / net price in the offer under consideration) * 100

The total price must be given in net and gross value, broken down into the value of individual tasks, must be given in the currency specified in the Form of Offer.
The price in the offer must include all costs and components related to the performance of the contract and the conditions set by the Ordering Party. Price variants are not allowed.
If the bids are received in different currencies, the Ordering Party will, for the purposes of evaluating the bids, convert the bid amount into PLN at the average exchange rate of the National Bank of Poland on the last day for submitting bids.

The performance of the contract will be entrusted to the Offerer who obtained the highest total number of points.

D) The method of preparing the offer

The offerer may submit one offer in writing, in Polish and / or English. If an offer is submitted in both languages, the Polish version will be binding.
The offer and the required attachments submitted with the offer require the signature of persons authorized to represent the company in business transactions, in accordance with the registration act and legal provisions.
Documents should be prepared in accordance with the recommendations and templates provided by the Ordering Party, and contain information and data specified in these documents.
Amendments to the offer must be legible and signed by the person / persons signing the offer.
In order to make it easier to read the content of the offer, it is recommended that all pages of the offer be numbered and permanently connected.

E) Date and method of submitting offers

Offers should be submitted by: 25.01.2021, 12:00 p.m. to the e-mail address of the person authorized to contact the offerers. The title of the e-mail should include: "[NaviSoC2] Offer referring to request for Offer No 03/2020". Offers submitted after the deadline will not be assessed, as invalid.

The period of validity of the offer
The period of validity of the offer begins with the deadline for submitting offers. The offerer

remains bound by the offer for up to 5 days from the date of closing the call for tenders. In justified cases, the Ordering Party may ask the offerers for consent to extend this period for a specified period at least 2 days before the expiry of the tender validity. The Offerer may extend the offer validity period himself, notifying the Ordering Party about it.

F) Information on the scope of exclusion (in relation to relatedentities)

In order to avoid a conflict of interests, public contracts, with the exception of sectoral contracts, awarded by a beneficiary who is not an entity obliged to apply the Public Procurement Law in accordance with Article 3 of the Public Procurement Law, may not be awarded to entities related to them personally or by capital. Capital or personal links are understood as interrelationships between the beneficiary or persons authorized to incur liabilities on behalf of the beneficiary, activities related to the preparation and conduct of the Contractor selection procedure and the Contractor, consisting in particular of:
- related or being a subsidiary, jointly dependent or dominant entity in relation to the Beneficiary within the meaning of the Act of 29 September 1994 on accounting;
- being an entity remaining with the Beneficiary or members of their bodies in such a factual or legal relationship that may raise justified doubts as to the impartiality in choosing a supplier of goods or services, in particular those who are married, kinship or affinity up to the second degree, adoption , custody or guardianship, also through membership in the bodies of the supplier of goods or services;
- being a related entity or a partner entity in relation to the Beneficiary within the meaning of Regulation No. 651/2014;
- being an entity related personally to the Beneficiary within the meaning of Art. 32 sec. 2 of the Act of March 11, 2004 on tax on goods and services.

5. Specification of the conditions for amending the contract concluded as a result of the public procurement procedure

The Ordering Party provides for the possibility of changing the provisions of the concluded contract in relation to the content of the offer on the basis of which the Offerer was selected, in the following scope:

- Termination of the contract if the Ordering Party does not receive funding under the competition conducted by the National Center for Research and Development
- Changes to the contract performance schedule resulting from the provisions of the contract between the Ordering Party and the NCBiR, if the contract was concluded or amended with an annex after the contract was awarded
- Changes in the (gross) price resulting from the change in the applicable VAT regulations

6. Information on formalities that should be completed after selecting an offer in order to conclude a contract

1. The Ordering Party will confirm the acceptance of the offer of the Offerer who will submit the most advantageous offer, provided that funding is obtained for the implementation of the project.
2. If it turns out that the Offerer whose offer has been selected will not provide the

service in accordance with the terms of the offer, the Ordering Party may choose the offerer's offer, whose offer was considered the next best, unless there is no such possibility, then the procedure will be canceled.
3. The contracting authority may cancel the procedure if the price of the best offer exceeds the amount allocated for financing the contract.

7. Final provisions

The Ordering Party does not reimburse offerers for the costs of preparing offers and other costs of participation in the procedure.
All statements, applications, notifications and information shall be provided by the Ordering Party and offerers electronically.
In justified cases, the Ordering Party may modify the content of the request of offer before the deadline for submitting offers. Any modifications, additions and arrangements as well as changes, including changes of dates as well as offerers' questions with explanations, become an integral part of the inquiry and will be binding when submitting offers. All rights and obligations of the Offerer in relation to the previously agreed dates will be subject to the new date.

The results of the competition procedure will be published on the website: http://chipcraft-ic.com

The person authorized to contact the offerers:
Tomasz Borejko
e-mail: t.borejko@chipcraft-ic.com

8. List of attachments to the inquiry:

Attachment No 1 - Form of Offer
Attachment No 2 - Detailed description of the subject of the contract

Attachment No 2

Detailed description of the subject of the contract

The subject of the contract includes the purchase of commercial EDA / CAD software licenses for the design of integrated circuits

The subject of the order contains specialized computer software EDA/CAD tools-set for the integrated circuits design and implementation. Software must allow 36 months of work for the design of analog, mixed-signal and digital integrated circuits. The EDA/CAD software should work under the control of the Enterprise-class Linux operating system and must be compatible with the RHEL-64bit 6.x series or its clones (e.g. CentOS 6.x or Scientific Linux 6.x).

The software must work as an integrated package and allow a full flow design and verification of analog, mixed-signal and digital ICs. The package should contain the following tools:

- Schematic editor,
- Circuit simulator,
- Layout editor,
- Logic simulator,
- Complete automatic system for logic synthesis and Place & Route of digital IC and SoC, which covers full RTL-to-GDS flow,
- Formal equivalence checking tool,
- Clock tree optimization tool with clock concurrent optimization for DSM technologies,
- Design Rules Checker and Layout Versus Schematic checker,
- RC parasitic extraction tool.

Technical specification:

No.	Technical parameter	Required by the Employer
1.	General description	• EDA/CAD software toolset for integrated circuit design • The whole toolset must enable all design flow for full-custom design and verification of analog, mixed-signal and digital systems • The offered software toolset must be integrated, which means that toolset must work with one, unified project database (e.g. *OpenAccess - OA*) • The offered software must work with OA foundry's PDK for TSMC 40nm, 65nm, 180nm; HHGrace 90nm, 110nm; GF 22nm, 40nm, 55nm, X-Fab 130nm, 180nm; STM 28nm; VIS 110nm, 150nm; UMC 55nm, 130nm; LFoundry 110nm, 150nm nodes
2.	Schematic editor (e.g. *Virtuoso Schematic Editor L* or equivalent)	• The ability to run at least two independent editors at the same time - the possibility of simultaneous work of two users of the schematic editor • Support for hierarchical projects, which contains various cell-views representations of sub-systems and their models: electrical sub-schematics, Verilog VHDL and Verilog AMS • Hierarchical connection highlighting • Hierarchical search for connections and instances • Support for PDK's P-Cells (Parametrized Cells) provided in TSMC 40nm, 65nm, 180nm; HHGrace 90nm, 110nm; GF 22nm, 40nm, 55nm, X-Fab 130nm, 180nm; STM 28nm; VIS 110nm, 150nm; UMC

		55nm, 130nm; LFoundry 110nm, 150nm nodes
3.	Circuit simulator (e.g. *Spectre Multi-Mode Simulation with Spectre X* or equivalent) with integrated user interface (e.g. *Virtuoso ADE Explorer* or equivalent)	• Integrated with schematic GUI, which enables configuration setup and run of analog and AMS simulations • The ability to run at least three GUIs at the same time, which allow to run parameterized simulations, Process Corners and statistical Monte Carlo - the possibility of simultaneous work of three users of the graphical simulation environment GUI • SPICE-level circuit simulator • Fast-SPICE type circuit simulator for large IC (use of multiple processor cores in one simulation) • Analog and AMS simulator, which supports HDL's modelling: VHDL, VHDL-AMS, Verilog, SystemVerilog, Verilog-AMS • Dedicated analyses for simulation of analog and RFIC: DC Operating Point, small-signal AC, transient, noise and transient noise, stability analysis, harmonic balance and periodic steady-state • RF key parameters analysis: S-scattering matrix, impedance matching, stability, isolation, phase noise, inter-modulation distortion of third order intermodulation point IP3, 1dB gain compression, noise figure • Post-layout simulation with RC parasitic elements reduction • The ability to simultaneously run at least twelve basic SPICE simulations • The ability to simultaneously run at least six advanced Fast-SPICE or AMS simulations in multi-core
4.	Advanced-level, assisted layout editor (e.g. *Virtuoso Layout Suite XL* or equivalent)	• The ability to run at least three independent editors at the same time - the possibility of simultaneous work of three users of the layout editor • Design-rule–driven feature to automatically ensuring real-time process-design–rule correctness • Full support for P-Cells (Parametrized Cells) provided in TSMC 40nm, 65nm, 180nm; HHGrace 90nm, 110nm; GF 22nm, 40nm, 55nm, X-Fab 130nm, 180nm; STM 28nm; VIS 110nm, 150nm; UMC 55nm, 130nm; LFoundry 110nm, 150nm nodes • Hierarchical search for connections, instances and pins • Support for multi-part paths for to draw buses and shielded paths • Automated generation of layout device instances from schematic editor • Connectivity driven layout: cross-probe schematics and layout to highlight instances and devices, as well as quick identification of unconnected or shorted nets with theirs names • Constraint-driven layout environment to enforce user while generating layout and automatically flag and log constraint violations
5.	Logic simulator (e.g. *Xcelium Limited Single-Core* or equivalent)	• Hardware Description Language support: Verilog, VHDL, SystemVerilog, SystemC, PSL, Si2 Common Power Format (CPF) • GUI for analyzing and displaying results with debugging environment with scripting support in the TCL language
6.	Design Rules Checker (e.g. *Physical Verification System Design Rule Checker XL* or equivalent) and Layout Versus Schematic checker (*Physical Verification System Layout vs. Schematic Checker XL* or	• The ability to run at least three results browser GUIs at the same time and the possibility of simultaneous running of two DRC engines and one LVS engine simultaneously • The DRC and LVS tools must work with run-decks provided in TSMC 40nm, 65nm, 180nm; HHGrace 90nm, 110nm; GF 22nm, 40nm, 55nm, X-Fab 130nm, 180nm; STM 28nm; VIS 110nm, 150nm; UMC 55nm, 130nm; LFoundry 110nm, 150nm nodes • GUI debug environment integrated with the layout and schematic editors: interactive short locator, error results visualization, explanation

	equivalent)	and fixing
7.	RC parasitic extraction tool (e.g., *Quantus QRC Extraction – XL* or equivalent)	• The tools must work with run-decks provided in TSMC 40nm, 65nm, 180nm; HHGrace 90nm, 110nm; GF 22nm, 40nm, 55nm, X-Fab 130nm, 180nm; STM 28nm; VIS 110nm, 150nm; UMC 55nm, 130nm; LFoundry 110nm, 150nm nodes • RC extractor must to fully integrate with LVS engine and theirs runs results • Distributed Processing for multi-cpu support • Unlimited transistors and cell Instances • Multiple Process Corners • RC extraction with 3D Field Solver for 110 nm node
8.	Complete automatic system for logic synthesis and Place & Route of digital IC and SoC, which cover full RTL-to-GDS flow (e.g. *Genus Synthesis Solution* and *Innovus Implementation System* or equivalent)	• Logic synthesis with unlimited placeable instances number • P&R with unlimited placeable instances number • HDL support: Verilog, SystemVerilog, VHDL • Standard cell library supported formats: .alf, TLF end .lib • Support for abstracts in LEF format • SDC support • Support for exporting/importing: DEF, Verilog, RC parasitic in DSPF, SPICE and SPEF, SDF delay file, GDSII • Low power synthesis and implementation capabilities: multi-Vt MOS, clock and power gating. • SST and MMMC • Signal Integrity support by integrated tools for Signoff Timing Analysis (e.g. *Tempus Timing Signoff Solution L* or equivalent) • IR drop analysis support by integrated tools for Signoff Power Analysis (e.g. *Voltus IC Power Integrity Solution - L* or equivalent) • ATPG, Scan Compression insertion, OPCG, SmartScan, Ultra LPCT for on-wafer testing (e.g. *Modus ATPG* with *Modus DFT Option* or equivalent) • Full custom (e.g. *OpenAccess*) database support for data exchange between digital and analog/AMS environment • Distributed Processing for multi-cpu support • Tools (8) must allow quarterly work during the 36 months period of the (2-7) license period three times (three quarters of usage)
9.	Formal equivalence checking tool (e.g. *Conformal Low Power – XL* or equivalent)	• HDL support: Verilog, SystemVerilog, VHDL • SPICE type netlist support • Support for .lib format • Support for dynamic and static power synthesis optimizations such as clock gating and signal gating, multi-Vt libraries • Common Power Format (CPF) support • Tool (9) must allow quarterly work during the 36 months period of the (2-7) license period two times (two quarters of usage)
10.	Clock tree optimization tool with clock concurrent optimization for DSM technologies (e.g. *Encounter Clock Concurrent Optimization* or equivalent)	• Distributed Processing for multi-cpu support • Implementation clock tree as H-tree topology • Decreasing IR drop • Tool (10) must allow quarterly work during the 36 months period of the (2-7) license period two times (two quarters of usage)

COMMENTS:

1. In the event that proprietary names / reference brands are used in the Request for Offer, it should be understood that the order concerns a product or a product component not worse than the name / brand indicated.