

LOW-DROPOUT VOLTAGE REGULATOR

Name		Description	
CCLDO2V5TOL5V5N40A		Low-Dropout Voltage Regulator generating 2.5 V with a maximum load of 30 mA and a supply voltage tolerance of 5.5V	
Category		Type	Status
Power Management		LDO	GDS
Foundry	Technology	Process Node	Year
TSMC	CMOS	40 nm	2025
Deliverables (preferable IP merge model)			
<ul style="list-style-type: none"> ◆ Datasheet ◆ Characterization report ◆ Encrypted Flat Extracted netlist with parasitic ◆ Behavioral models 		<ul style="list-style-type: none"> ◆ Abstract View ◆ Timing View ◆ DRC, LVS and antenna report ◆ Integration guidelines and support 	

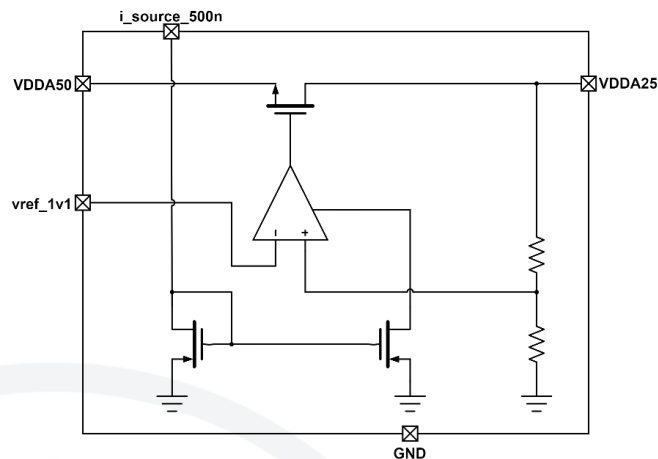


Figure 1. Simplified block diagram.

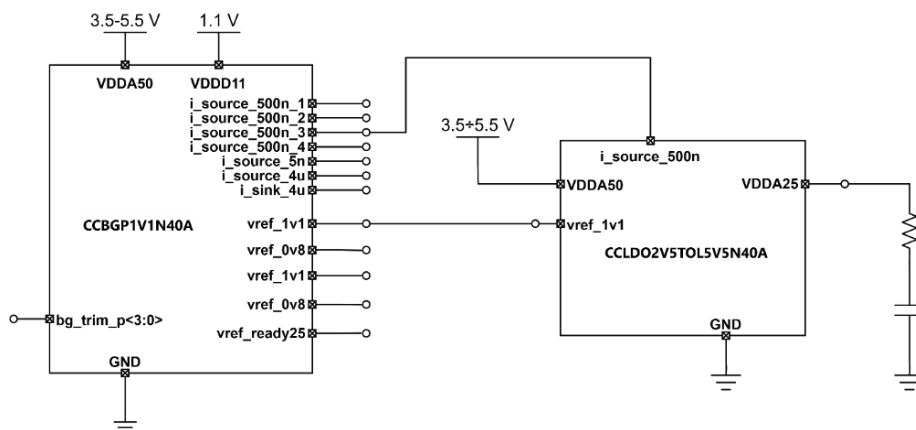


Figure 2. Typical use case.

Table 1. Pin description.

Pin name	Direction	Type	Active	Description
VDDA50	I/O	Power		5.0 V power supply voltage, tolerance 3.5 V to 5.5 V
VDDA25	I/O	Power		Generated by LDO 2.5 V power supply voltage, tolerance 2.25 V to 2.75 V
GND	I/O	Power		Ground
I_source_500n	I/O	Analog		Input bias current 500 nA supplied by external current source. Current should be supplied from PMOS current mirror
vref_1v1	I	Analog		1.1 V reference voltage input

Table 2. Specification.

Parameter	Description	Min.	Typ.	Max.	Unit
T_j	Operating junction temperature	-40	27	85	°C
VDDA50	IO Supply voltage	3.5	5.0	5.5	V
VDDD11	Core supply voltage	2.25	2.5	2.75	V
V_{ref}	Reference voltage	1.05	1.1	1.15	V
I_{load}	Load current			30	mA
C_{load}	External capacitor	4.7	10		μF
I_Q	Quiescent current consumption		2.17	2.86	μA
PSRR	Power Supply Rejection Ratio at 1MHz	30	57		dB
Load regulation	$\Delta V_{DDA25} / \Delta I_{load}$		1.4	1.8	V/A