

LOW-DROPOUT VOLTAGE REGULATOR

Name		Description		
CCLDO1V11A40A		Low-Dropout Voltage Regulator generating 1.1 V with a maximum load of 1A		
Category		Type	Status	
Power Management		LDO	GDS	
Foundry	Technology	Process Node	Year	
TSMC	CMOS	40 nm	2024	
Deliverables (preferable IP merge model)				
<ul style="list-style-type: none"> ◆ Datasheet ◆ Characterization report ◆ Encrypted Flat Extracted netlist with parasitic ◆ Behavioral models 		<ul style="list-style-type: none"> ◆ Abstract View ◆ Timing View ◆ DRC, LVS and antenna report ◆ Integration guidelines and support 		

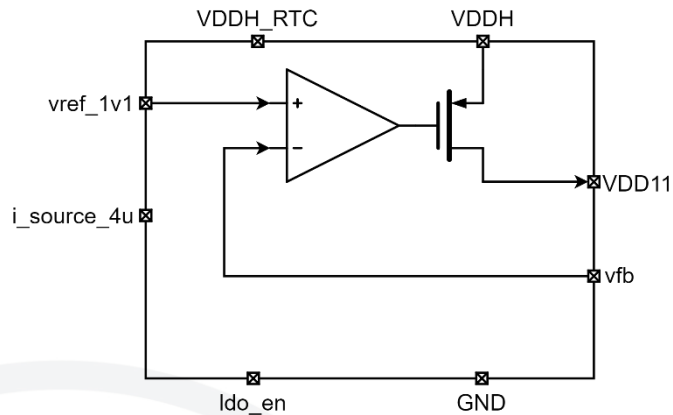


Figure 1. Simplified block diagram.

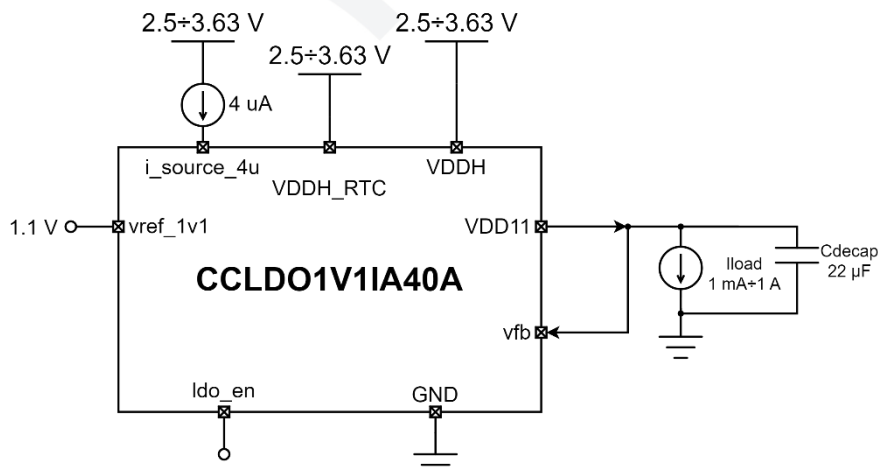


Figure 2. Typical use case.

Table 1. Pin description.

Pin name	Direction	Type	Active	Description
VDDH	I/O	Power		Power supply voltage, tolerance 2.5 V to 3.63 V
VDDH_RTC	I/O	Power		Power supply voltage for RTC LDO
VDD11	I/O	Power		1.1 V Output LDO Voltage
GND	I/O	Power		Ground
vfb	I/O	Analog		Feedback voltage to OTA
i_source_4u	I/O	Analog		Input bias current 4 μ A supplied by external current source. Current should be supplied from PMOS current mirror.
vref_1v1	I/O	Analog		Positive 1.1 V reference voltage output
ldo_en	I	Digital	High	Enable signal in 3.3 V domain

Table 2. Specification.

Parameter	Description	Min.	Typ.	Max.	Unit
T_j	Operating junction temperature	-40	27	125	$^{\circ}$ C
V_{DDH}	Input voltage	2.5	3.3	3.63	V
I_{source}	Input reference current $\pm 10\%$ accurate	3.6	4	4.4	μ A
V_{ref}	Input reference voltage		1.1		V
V_{DD11}	Output voltage (including PVT variation) (+ -10%)	1.05	1.1	1.15	V
I_{load}	Load current @ $V_{in} = 2.5$ V			300	mA
	Load current @ $V_{in} \geq 3$ V			1000	mA
C_{load}	Output capacitive load	22			μ F
I_Q	Quiescent current consumption			30	μ A
PSRR	@1 kHz, $C_L=22$ μ F			-26	dB
	@1 MHz, $C_L=22$ μ F			-34	dB
V_{DD11_load}	Load regulation: $\Delta V_{DD11}/\Delta I_{load}$	50		100	mV/A