

# 14-BIT 200 MSPS ADC

Name		Description	
CCGADC14B200M40A		GNSS IF 14-bit 200 Msp/s Analog-to-Digital Converter	
Category		Type	Status
Data Converters		ADC	In Development
Foundry	Technology	Process Node	Year
TSMC	CMOS	40 nm	2024
Deliverables (preferable IP merge model)			
<ul style="list-style-type: none"> <li>◆ Datasheet</li> <li>◆ Characterization report</li> <li>◆ Encrypted Flat Extracted netlist with parasitic</li> <li>◆ Behavioral models</li> </ul>		<ul style="list-style-type: none"> <li>◆ Abstract View</li> <li>◆ Timing View</li> <li>◆ DRC, LVS and antenna report</li> <li>◆ Integration guidelines and support</li> </ul>	

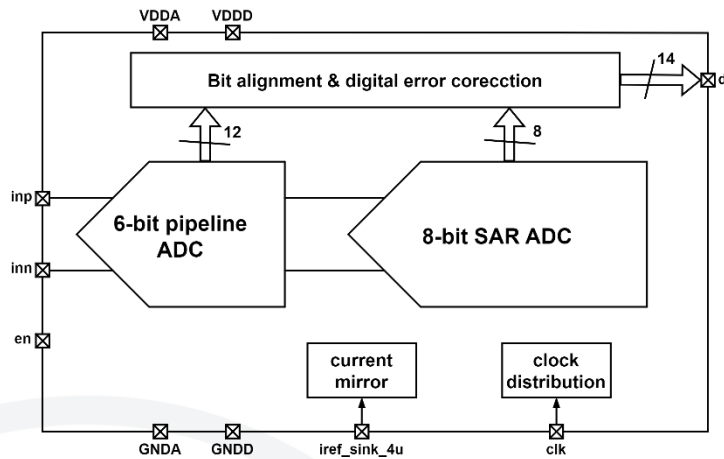


Figure 1. Simplified block diagram.

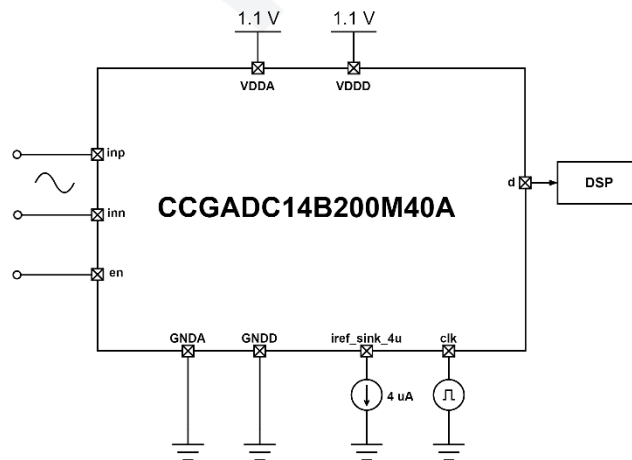


Figure 2. Typical use case.

Table 1. Pin description.

Pin name	Direction	Type	Active	Description
inp	I	Analog		Positive input voltage signal
inn	I	Analog		Negative input voltage signal
d<13:0>	O	Digital		Output 14-bit word
iref_sink_4u	I/O	Analog		4 uA reference current
en	I	Digital	High	Enable signal
clk	I	Digital		Digital clock signal
GNDA	I/O	Power		Analog Ground
GNDD	I/O	Power		Digital Ground
VDDA	I/O	Power		1.1 V Analog Supply
VDDD	I/O	Power		1.1 V Digital Supply

Table 2. Specification.

Parameter	Description	Min.	Typ.	Max.	Unit
T <sub>j</sub>	Operating junction temperature	-40	27	125	°C
VDDA	Supply voltage	0.99	1.1	1.21	V
VDDD	Supply voltage	0.99	1.1	1.21	V
I <sub>ref</sub>	Reference current		4		uA
Missing codes			No		-
DNL	Differential nonlinearity	-1.0		1.0	-
INL	Integral nonlinearity	-1.0		1.0	-
f <sub>clk</sub>	Maximum clock frequency	200			MHz
FS	Input Differential Full scale amplitude	608.4	676	743.6	mV
ENOB	Effective number of bits for full-scale input	12			-
SNR	Signal-to-Noise ratio	74.7			dBFS
SNDR	Signal-to-Noise-and-Distortion Ratio	74			dBFS
SFDR	Spurious free Dynamic Range			84.3	dB
Noise Density		-163.5			dBFS/Hz
THD	Total Harmonic Distortion			-82.3	dBc
I <sub>off</sub>	Current power-down drawn			10	nA
I <sub>c</sub>	Current consumption			25	mA