

# STEP-DOWN DCDC CONVERTER

Name		Description	
CCDCDC1V1I1A40A		1.1V step-down DC-DC converter with a maximum load of 1A	
Category		Type	Status
Power Management		DCDC	GDS
Foundry	Technology	Process Node	Year
TSMC	CMOS	40 nm	2024
Deliverables (preferable IP merge model)			
<ul style="list-style-type: none"> <li>◆ Datasheet</li> <li>◆ Characterization report</li> <li>◆ Encrypted Flat Extracted netlist with parasitic</li> <li>◆ Behavioral models</li> </ul>		<ul style="list-style-type: none"> <li>◆ Abstract View</li> <li>◆ Timing View</li> <li>◆ DRC, LVS and antenna report</li> <li>◆ Integration guidelines and support</li> </ul>	

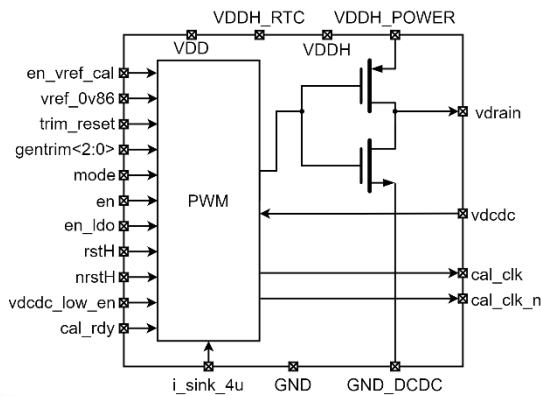


Figure 1. Simplified block diagram.

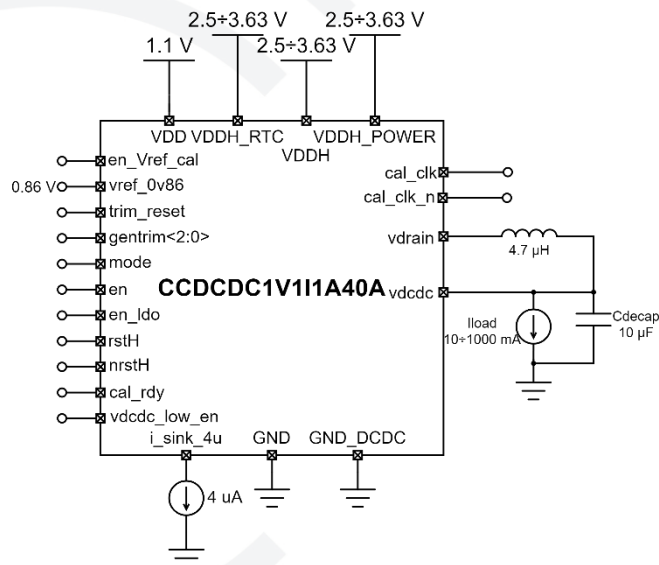


Figure 2. Typical use case.

Table 1. Pin description.

Pin name	Direction	Type	Active	Description
VDD	I/O	Power		1.1 V power supply
VDDH_RTC	I/O	Power		3.3 V high voltage power supply for RTC
VDDH	I/O	Power		3.3 V high voltage power supply for DCDC control loop
VDDH_POWER	I/O	Power		3.3 V high voltage power supply for power PMOS transistor
GND	I/O	Power		Ground for DCDC control loop
GND_DCDC	I/O	Power		DCDC Ground, connected to power NMOS
vdrain	I/O	Power		DCDC output, connected to inductor
vdcdc	I/O	Power		DCDC output voltage, connected to control loop
cal_clk	O	Digital		Clock signal for reference voltage calibration
cal_clk_n	O	Digital		Negative clock signal for reference voltage calibration
i_sink_4u	I/O	Analog		Input 4 $\mu$ A bias current, fed from NMOS current mirror
en_vref_cal	I	Digital	High	Enabling reference voltage calibration mode
vref_0v86	I	Analog		0.86 V voltage reference for error amplifier
trim_reset	I	Digital		DCDC frequency trimming enable: '0' – Flash, '1' – configuration register
gentrim<2:0>	I	Digital		DCDC frequency trimming value
mode	I	Digital		DCDC work mode: '0' – Voltage mode, '1' – Current mode
en	I	Digital	High	DCDC enable signal
en_ldo	I	Digital	High	LDO enable signal
rstH	I	Digital	High	Level shifters reset signal
nrstH	I	Digital	Low	Level shifters reset signal, negated
vdcdc_low_en	I	Digital	High	Switch DCDC output voltage to 0.9 V
cal_rdy	I	Digital	High	Reference voltage calibration is completed

Table 2. Specification.

Parameter	Description	Min.	Typ.	Max.	Unit
$T_j$	Operating junction temperature	-40	27	85	°C
$V_{DDH}$	Input voltage	2.5	3.3	3.63	V
$V_{dcdc}$	Output voltage (including PVT variation) (+ -10%)	1.05	1.1	1.15	V
$V_{DD}$	Core power voltage		1.1		V
$I_{out}$	Load current	10		1000	mA
$\eta$	Energy efficiency at $I_{out}=300$ mA	85			%
$V_{out\_ripple}$	Output voltage ripple (pk-pk)			100	mV
$C_{load}$	Decoupling capacitor	10			$\mu$ F
L	DCDC inductor		4.7		$\mu$ H
$V_{ref}$	Input voltage reference		0.86		V
$F_{sw}$	Switching frequency		900		kHz