

# SYSTEM-ON-CHIP IP PACKAGE FOR 32-BIT RISC-V PROCESSOR CORE

Name	Description	
CC-RV32xx-S	System-on-Chip IP Package for 32-bit RISC-V Processor Core	
Category	Type	Status
RISC-V Cores	RISC-V	Silicon and FPGA Proven
Deliverables		
<ul style="list-style-type: none"> <li>◆ RTL code</li> <li>◆ User manual</li> <li>◆ Integration manual</li> </ul>	<ul style="list-style-type: none"> <li>◆ Testbench</li> <li>◆ SDK/IDE</li> <li>◆ Support</li> </ul>	
Features		
<ul style="list-style-type: none"> <li>◆ High Performance 32-bit RISC-V CPU</li> <li>◆ Proprietary 6-stage pipeline</li> <li>◆ PHT, GHR, BTB branch prediction</li> <li>◆ RV32GCX instruction set</li> <li>◆ Single or multicore implementation</li> <li>◆ Up to 1.51 DMIPS/MHz/Core</li> <li>◆ Up to 2.51 CoreMark/MHz/Core</li> <li>◆ Associative caches with snooping and parity</li> <li>◆ 32, 64, 128 bit main bus width</li> </ul>	<ul style="list-style-type: none"> <li>◆ Custom instruction set extension</li> <li>◆ Power-down mode</li> <li>◆ On-chip debug support</li> <li>◆ Separate or joint Instruction/Data interface</li> <li>◆ JTAG and UART Debug Link</li> <li>◆ Free GNU-Based C/GDB toolchain</li> <li>◆ Cycle accurate simulator</li> <li>◆ Technology independent IP Core</li> <li>◆ Flexible licensing scheme</li> </ul>	

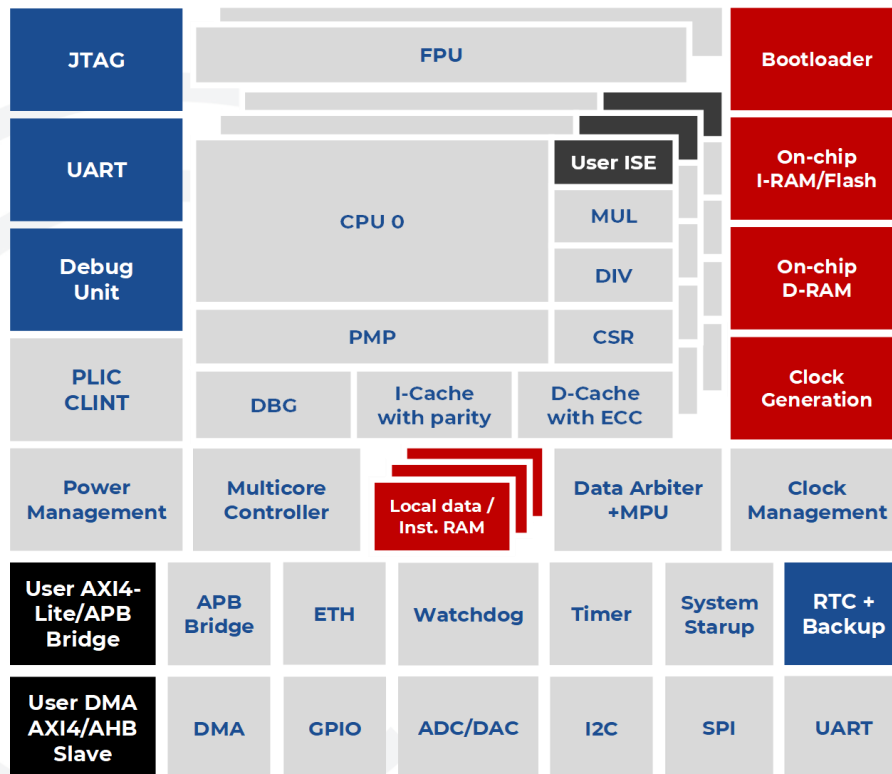


Figure 1. Simplified block diagram.