CONFIGURABLE WATCHDOG TIMER

Name	Description	
CC-WDT-APB	Configurable Watchdog Timer with APB Interface	
Category	**Type**	**Status**
MCU Peripherals	Watchdog	Silicon and FPGA Proven
Deliverables		
♦ Unencrypted RTL code ♦ User manual ♦ Testbench	♦ C header file ♦ Support	
Features		
♦ AMBA APB3 bus ♦ Configurable timeout interval ♦ Standard and windowed mode ♦ Stop in debug mode option ♦ Register write protection	♦ Fully synthesizable synchronous design with positive edge clocking ♦ DFT ready ♦ Technology independent IP Core ♦ Flexible licensing scheme	

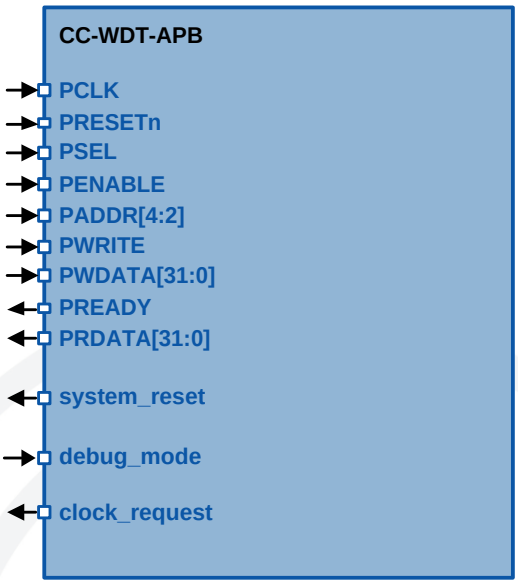
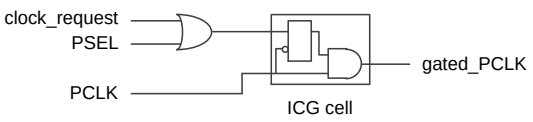
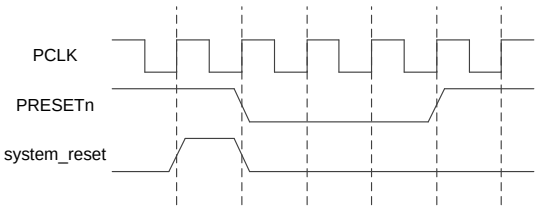


Figure 1. Symbol.



a) Using clock_request pin for low power mode



b) Timing of reset synchronizer connected to system_reset pin

Figure 2. Integration example.

ChipCraft Sp. z o.o.
Bukowinska 22 lok. 9B
02-703 Warsaw, POLAND

www.chipcraft-ic.com

Table 1. Pin description.

Pin name	Direction	Active	Description
PCLK	I	rising	Synchronous clock
PRESETn	I	low	Asynchronous reset
PSEL	I	high	APB peripheral select
PENABLE	I	high	APB bus enable
PADDR[4:2]	I	data	APB bus address
PWRITE	I	high	APB bus write
PWDATA[31:0]	I	data	APB bus write data
PREADY	O	high	APB bus ready
PRDATA[31:0]	O	data	APB bus read data
system_reset	O	high	Watchdog system reset output
debug_mode	I	high	Debug mode input
clock_request	O	high	Clock request signal

Table 2. Generic Parameters.

Generic name	Type	Range	Description
watchdog_width	integer	1:32	Watchdog timer width
prescaler_width	integer	1:32	Watchdog timer prescaler width

Table 3. Resource utilization.

Configuration	ASIC Gates [GE]
typical	1000