UART CONTROLLER

Name	Description	
CC-UART-APB	UART Controller with APB Interface	
Category	**Type**	**Status**
Serial/Parallel Interfaces	UART	Silicon and FPGA Proven

Deliverables

- Unencrypted RTL code
- User manual
- Testbench
- C header file
- Support

Features

- UART-compatible interface
- AMBA APB3 bus
- Full duplex
- Custom baud rate generation
- 8x, 16x oversampling
- 5, 6, 7, 8, 9 bits data
- 1, 2 stop bits
- LSB or MSB mode
- Configurable parity
- Hardware flow control
- RS485 mode
- Maskable interrupts
- Dedicated upstream and downstream
- DMA interface
- Fully synthesizable synchronous design with positive edge clocking
- DFT ready
- Technology independent IP Core
- Flexible licensing scheme

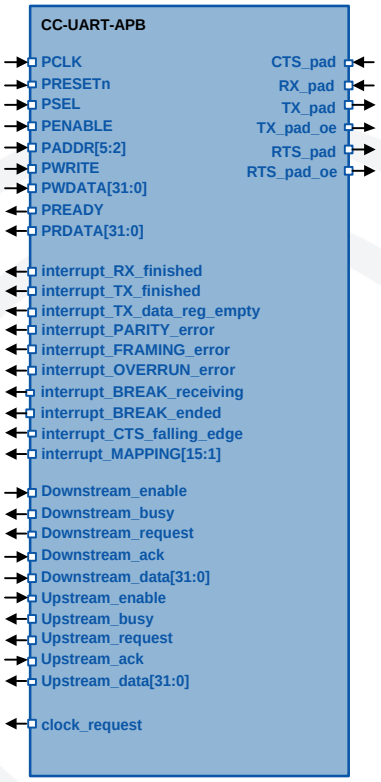
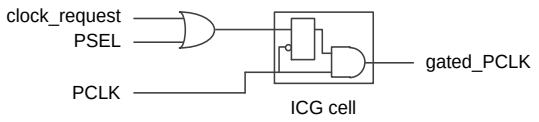
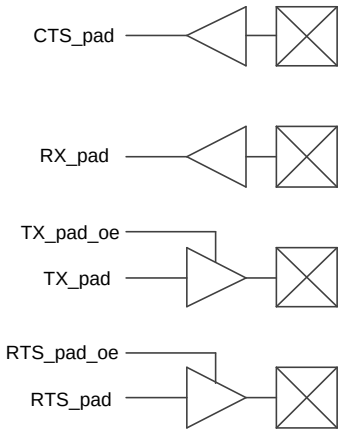


Figure 1. Symbol.



a) Using clock_request pin for low power mode



b) Pad connection example

Figure 2. Integration example.

ChipCraft Sp. z o.o.
Bukowinska 22 lok. 9B
02-703 Warsaw, POLAND

www.chipcraft-ic.com

Table 1. Pin description.

Pin name	Direction	Active	Description
PCLK	I	rising	Synchronous clock
PRESETn	I	low	Asynchronous reset
PSEL	I	high	APB peripheral select
PENABLE	I	high	APB bus enable
PADDR[5:2]	I	data	APB bus address
PWRITE	I	high	APB bus write
PWDATA[31:0]	I	data	APB bus write data
PREADY	O	high	APB bus ready
PRDATA[31:0]	O	data	APB bus read data
interrupt_RX_finished	O	high	Reception finished interrupt
interrupt_TX_finished	O	high	Transmission finished interrupt
interrupt_TX_data_reg_empty	O	high	Transmit data register empty interrupt
interrupt_PARITY_error	O	high	Parity error interrupt
interrupt_FRAMING_error	O	high	Framing error interrupt
interrupt_OVERRUN_error	O	high	Overrun error interrupt
interrupt_BREAK_receiving	O	High	Break receiving interrupt
interrupt_BREAK_ending	O	high	Break ended interrupt
interrupt_CTS_falling_edge	O	high	CTS falling edge interrupt
interrupt_MAPPING[15:1]	O	data	Interrupt mapping vector
Downstream_enable	I	high	PDMA downstream enable signal
Downstream_busy	O	high	PDMA downstream busy signal
Downstram_request	O	high	PDMA downstream request signal
Downstream_ack	I	high	PDMA downstream ack signal
Downstream_data[31:0]	I	data	PDMA downstream data
Upstream_enable	I	high	PDMA upstream enable signal
Upstream_busy	O	high	PDMA upstream busy signal
Upstram_request	O	high	PDMA upstream request signal
Upstream_ack	I	high	PDMA upstream ack signal
Upstream_data[31:0]	O	data	PDMA upstream data
clock_request	O	high	Clock request signal
CTS_pad	I	low	UART Clear To Send
RX_pad	I	data	UART Receive Input
TX_pad	O	data	UART Transmit Output
TX_pad_oe	O	high	UART TX output enable
RTS_pad	O	low/high	UART Ready To Send
RTS_pad_oe	O	high	UART RTS output enable

Table 2. Generic Parameters.

Generic name	Type	Range	Description
PDMA_support	integer	0, 1	Configure PDMA interface support
default_interrupt_MAPPING	integer	0:32767	Reset value of interrupt_MAPPING register