CONFIGURABLE TIMER COUNTER

Name	Description	
CC-TIMER-APB	Configurable Timer Counter with APB Interface	
Category	**Type**	**Status**
MCU Peripherals	TIMER	Silicon and FPGA Proven

Deliverables

- Unencrypted RTL code
- User manual
- Testbench
- C header file
- Support

Features

- AMBA APB3 bus
- Programmable multi-function timer
- Double buffered configuration registers
- Configurable single/dual slope PWM outputs
- Configurable standard/period/pulse input capture mode
- Stop in debug mode option
- Fully synthesizable synchronous design with positive edge clocking
- DFT ready
- Technology independent IP Core
- Flexible licensing scheme

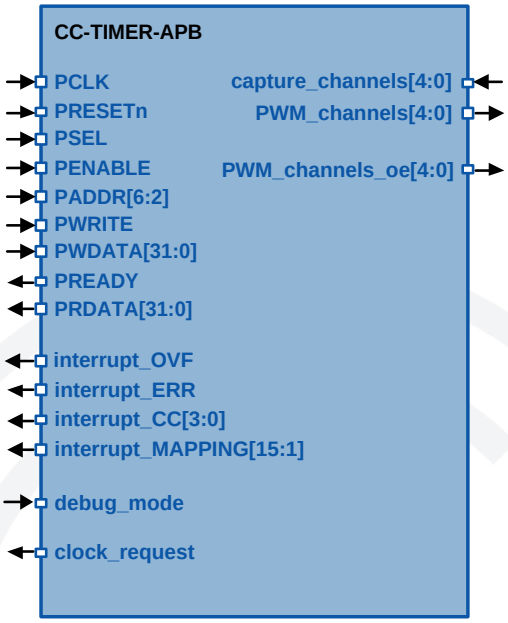
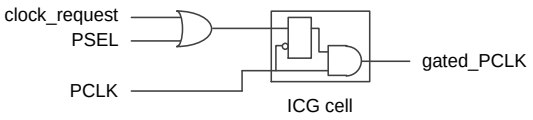
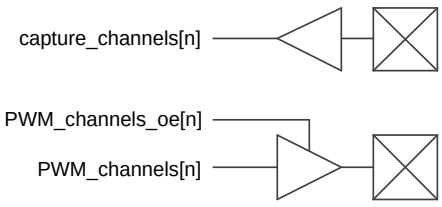


Figure 1. Symbol.



a) Using clock_request pin for low power mode



b) Pad connection example

Figure 2. Integration example.

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Table 1. Pin description.

Pin name	Direction	Active	Description
PCLK	I	rising	Synchronous clock
PRESETn	I	low	Asynchronous reset
PSEL	I	high	APB peripheral select
PENABLE	I	high	APB bus enable
PADDR[address_width+1:2]	I	data	APB bus address
PWRITE	I	high	APB bus write
PWDATA[31:0]	I	data	APB bus write data
PREADY	O	high	APB bus ready
PRDATA[31:0]	O	data	APB bus read data
capture_channels [cc_channels_number:0]	I	data	Timer capture inputs
PWM_channels [cc_channels_number:0]	O	data	Timer PWM outputs
PWM_channels_oe [cc_channels_number:0]	O	high	Timer PWM output enable
interrupt_OVF	O	high	Timer overflow interrupt
interrupt_ERR	O	high	Capture mode error interrupt
interrupt_CC [cc_channels_number:0]	O	high	Capture/compare interrupt
interrupt_MAPPING[15:1]	O	data	Interrupt mapping vector
debug_mode	I	high	Debug mode input
clock_request	O	high	Clock request signal

Table 2. Generic Parameters.

Generic name	Type	Range	Description
timer_width	integer	1:32	Timer counter width
prescaler_width	integer	1:32	Timer prescaler width
address_width	integer	1:32	APB PADDR signal width
cc_channels_number	integer	0:4	Number of capture/compare channels
default_interrupt_MAPPING	integer	0:32767	Reset value of interrupt_MAPPING register

Table 3. Resource utilization.

Configuration	ASIC Gates [kGE]
timer_width=16, cc_channels_number=0	1.0
timer_width=32, cc_channels_number=0	1.8
timer_width=16, cc_channels_number=2	2.0.
timer_width=32, cc_channels_number=4	4.9

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