SERIAL PERIPHERAL INTERFACE MASTER/SLAVE

Name	Description	
CC-SPI-APB	Serial Peripheral Interface Master/Slave with APB Interface	
Category	**Type**	**Status**
Serial/Parallel Interfaces	SPI	Silicon and FPGA Proven

Deliverables

- Unencrypted RTL code
- User manual
- Testbench
- C header file
- Support

Features

- SPI-compatible interface
- AMBA APB3 bus
- Master or slave mode
- Full duplex
- Programmable clock rate up to PCLK/2
- Slave speed up to PCLK/8
- Up to 8 slave select lines
- Slave MISO output enable generation for multiple slaves
- Configurable clock polarity and phase
- LSB or MSB mode
- 8, 16, 24, 32 bits data transfer mode
- Maskable interrupts
- Dedicated upstream and downstream
- DMA interface
- Fully synthesizable synchronous design with positive edge clocking
- DFT ready
- Technology independent IP Core
- Flexible licensing scheme

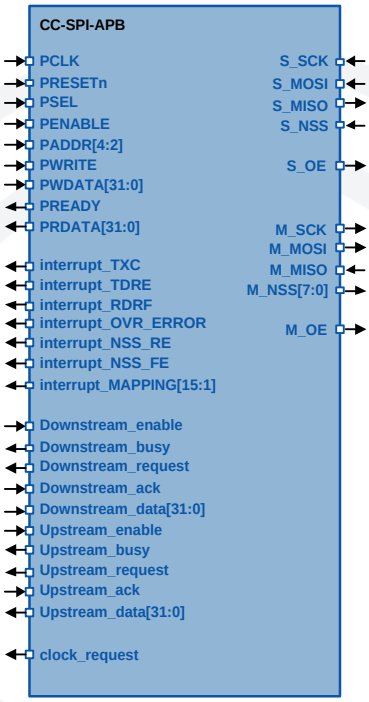
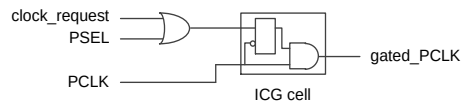
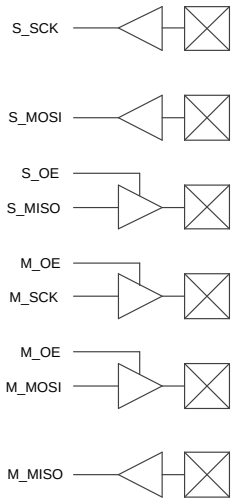


Figure 1. Symbol.



a) Using clock_request pin for low power mode



b) Pad connection example

Figure 2. Integration example.

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Table 1. Pin description.

Pin name	Direction	Active	Description
PCLK	I	rising	Synchronous clock
PRESETn	I	low	Asynchronous reset
PSEL	I	high	APB peripheral select
PENABLE	I	high	APB bus enable
PADDR[4:2]	I	data	APB bus address
PWRITE	I	high	APB bus write
PWDATA[31:0]	I	data	APB bus write data
PREADY	O	high	APB bus ready
PRDATA[31:0]	O	data	APB bus read data
interrupt_TXC	O	high	Transmission complete interrupt
interrupt_TDRE	O	high	Transmit data register empty interrupt
interrupt_RDRF	O	high	Read data register full interrupt
interrupt_OVR_ERROR	O	high	Overrun interrupt
interrupt_NSS_RE	O	high	NSS rising edge interrupt
interrupt_NSS_FE	O	high	NSS falling edge interrupt
interrupt_MAPPING[15:1]	O	data	Interrupt mapping vector
Downstream_enable	I	high	PDMA downstream enable signal
Downstream_busy	O	high	PDMA downstream busy signal
Downstram_request	O	high	PDMA downstream request signal
Downstream_ack	I	high	PDMA downstream ack signal
Downstream_data[31:0]	I	data	PDMA downstream data
Upstream_enable	I	high	PDMA upstream enable signal
Upstream_busy	O	high	PDMA upstream busy signal
Upstram_request	O	high	PDMA upstream request signal
Upstream_ack	I	high	PDMA upstream ack signal
Upstream_data[31:0]	O	data	PDMA upstream data
clock_request	O	high	Clock request signal
S_SCK_pad	I	rising or falling	SPI Slave clock
S_MOSI_pad	I	data	SPI Slave Master Out/Slave In
S_NSS_pad	I	low	SPI Slave serial select
S_MISO_pad	O	data	SPI Slave Master In/Slave Out
S_OE	O	high	SPI Slave output enable
M_MISO_pad	I	data	SPI Master Master In/Slave Out
M_SCK_pad	O	rising or falling	SPI Master clock
M_MOSI_pad	O	data	SPI Master Master Out/Slave In
M_NSS_pad[mss_number:0]	O	low	SPI Master serial select
M_OE	O	high	Master output enable

Table 2. Generic Parameters.

Generic name	Type	Range	Description
PDMA_support	integer	0, 1	Configure PDMA interface support
slave_support	integer	0, 1	Configure SPI slave support
default_interrupt_MAPPING	integer	0:32767	Reset value of interrupt_MAPPING register
mss_number	integer	0:8	Number of slave select pins

Table 3. Resource utilization.

Configuration	ASIC Gates [kGE]
slave_support=0, PDMA_support=1	2.7
slave_support=1, PDMA_support=1	4.0

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