SYSTEM-ON-CHIP IP PACKAGE FOR 32-BIT RISC-V PROCESSOR CORE

Name	Description	
CC-RV32xx-S	System-on-Chip IP Package for 32-bit RISC-V Processor Core	
Category	**Type**	**Status**
RISC-V Cores	RISC-V	Silicon and FPGA Proven
Deliverables		
♦ RTL code ♦ User manual ♦ Integration manual	♦ Testbench ♦ SKD/IDE ♦ Support	
Features		
♦ High Performance 32-bit RISC-V CPU ♦ Proprietary 6-stage pipeline ♦ PHT, GHR, BTB branch prediction ♦ RV32GCX instruction set ♦ Single or multicore implementation ♦ Up to 1.51 DMIPS/MHz/Core ♦ Up to 2.51 CoreMark/MHz/Core ♦ Set-associative caches with data snooping and parity	♦ Custom instruction set extension ♦ Power-down mode ♦ On-chip debug support ♦ Separate or joint Instruction/Data interface ♦ JTAG and UART Debug Link ♦ Free GNU-Based C/GDB toolchain ♦ Cycle accurate simulator ♦ Technology independent IP Core ♦ Flexible licensing scheme	

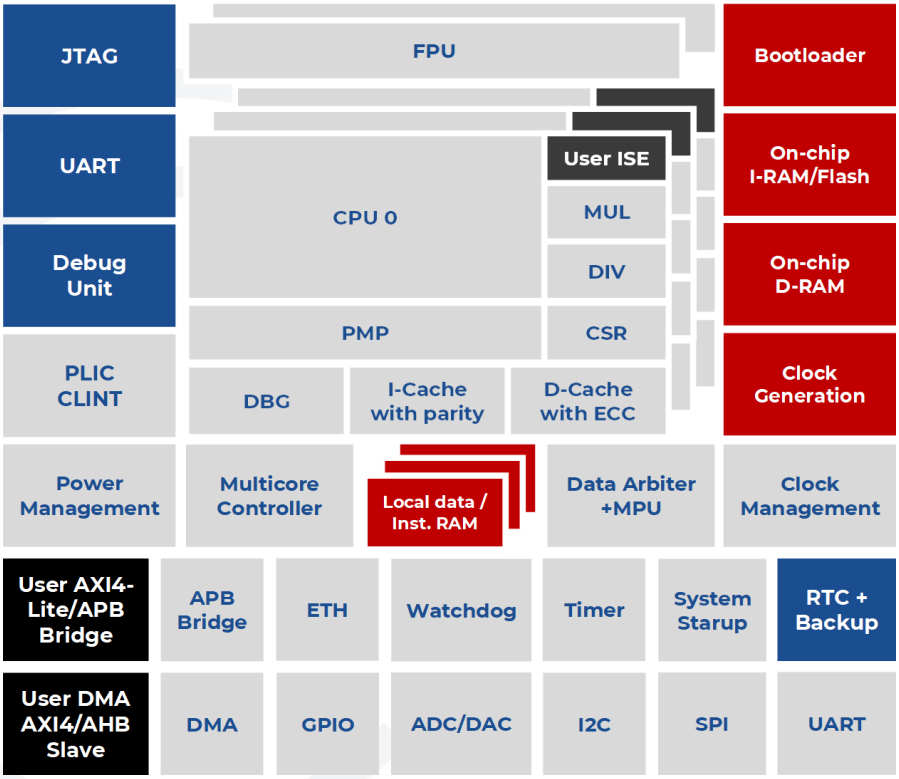

Figure 1. Simplified block diagram.

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