HIGH RELIABILITY 32-BIT RISC-V PROCESSOR CORE

Name	Description	
CC-RV32HR-C	High Reliability 32-bit RISC-V Processor Core	
Category	**Type**	**Status**
RISC-V Cores	RISC-V	Under Validation

Deliverables

- RTL code
- User manual
- Integration manual
- Software manual
- Testbench
- SDK/IDE
- Support

Features

- High Performance 32-bit RISC-V CPU
- Proprietary 6-stage pipeline
- RV32GCX instruction set
- Variable delayed dual-core lockstep operation
- Split dual-core mode for high-performance operation
- Up to 1.32 DMIPS/MHz/Core
- Up to 2.26 CoreMark/MHz/Core
- Custom instruction set extension
- Set-associative caches with data snooping and parity and ECC
- Power-down mode
- On-chip debug support
- Separate or joint Instruction/Data interface
- JTAG and UART Debug Link
- Free GNU-Based C/GDB toolchain
- Cycle accurate simulator
- Technology independent IP Core
- Flexible licensing scheme

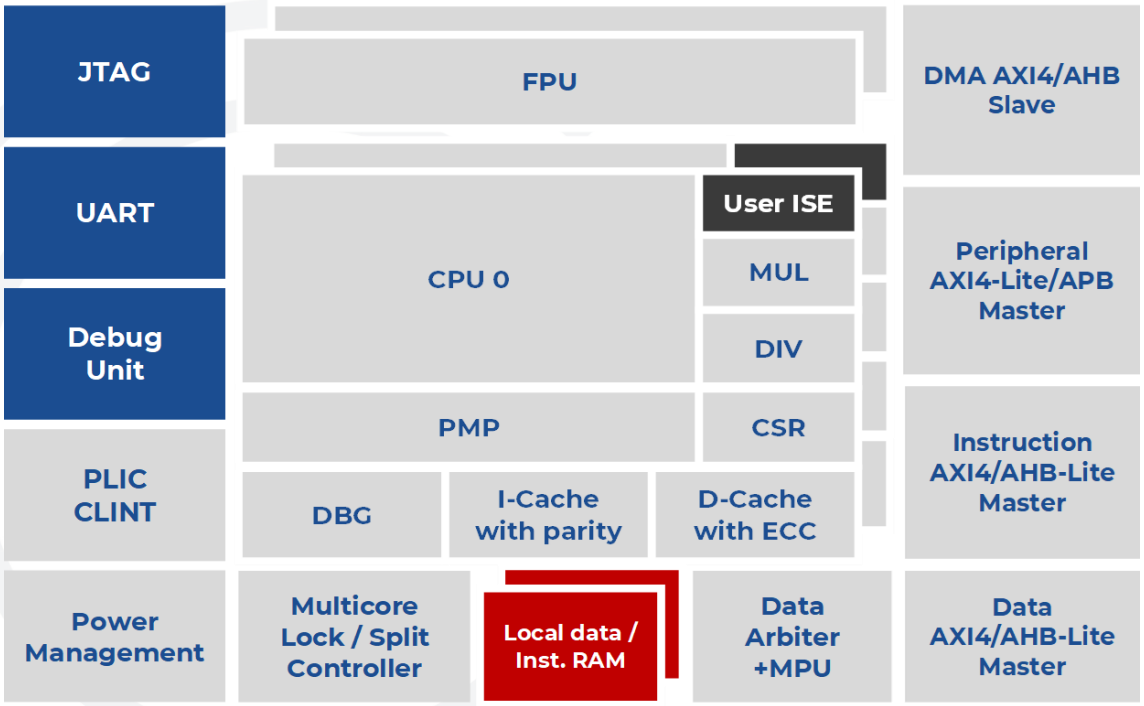

Figure 1. Simplified block diagram.

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