PROGRAMMABLE REAL TIME COUNTER

Name	Description	
CC-RTC-APB	Programmable Real Time Counter with APB Interface	
Category	**Type**	**Status**
MCU Peripherals	RTC	Silicon and FPGA Proven

Deliverables

- Unencrypted RTL code
- User manual
- Testbench
- C header file
- Support

Features

- AMBA APB3 bus
- Programmable multi-function RTC timer
- Configurable WKUP0 input
- Configurable SHDN output
- Maskable interrupts
- Timestamp generation
- User backup registers
- Backup RAM memory
- Fully synthesizable synchronous design with positive edge clocking
- DFT ready
- Technology independent IP Core
- Flexible licensing scheme

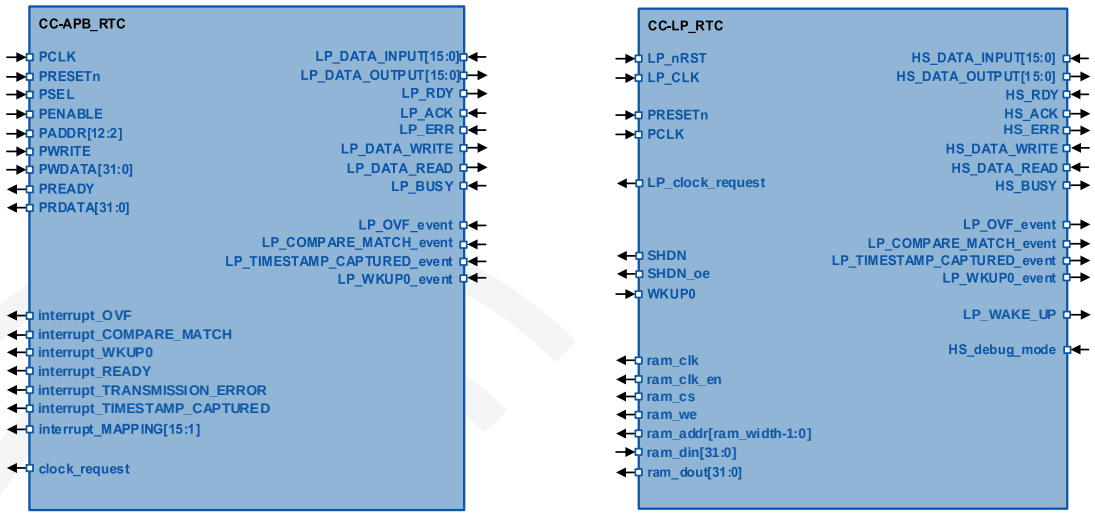

Figure 1. Symbols.

a) Using clock_request pin for low power mode

b) Pad connection example

Figure 2. Integration example.

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Table 1. CC-APB_RTC Pin description.

Pin name	Direction	Active	Description
PCLK	I	rising	Synchronous clock
PRESETn	I	low	Asynchronous reset
PSEL	I	high	APB peripheral select
PENABLE	I	high	APB bus enable
PADDR[12:2]	I	data	APB bus address
PWRITE	I	high	APB bus write
PWDATA[31:0]	I	data	APB bus write data
PREADY	O	high	APB bus ready
PRDATA	O	data	APB bus read data
LP_DATA_OUTPUT[15:0]	O	data	Data output
LP_DATA_INPUT[15:0]	I	data	Data input
LP_DATA_WRITE	O	high	Data write
LP_DATA_READ	O	high	Data read
LP_RDY	O	high	Data ready
LP_ACK	I	high	Data acknowledge
LP_ERR	I	high	Data error
LP_BUSY	I	high	Data busy
LP_OV_event	I	high	Overflow event
LP_COMPARE_MATCH_event	I	high	Compare match event
LP_WKUP0_event	I	high	WKUP0 event
LP_TIMESTAMP_CAPTURED_event	I	high	Timestamp captured event
interrupt_OVF	O	high	Overflow interrupt
interrupt_COMPARE_MATCH	O	high	Compare match interrupt
interrupt_WKUP0	O	high	WKUP0 interrupt
interrupt_READY	O	high	Ready interrupt
interrupt_TRANSMISSION_ERROR	O	high	Transmission error interrupt
interrupt_TIMESTAMP_CAPTURED	O	high	Timestamp captured interrupt
interrupt_MAPPING[15:1]	O	data	Interrupt mapping vector
clock_request	O	high	Clock request

Table 2. CC-LP_RTC Pin description.

Pin name	Direction	Active	Description
LP_nRST	I	low	Asynchronous low power reset
LP_CLK	I	rising	Synchronous low power clock
PRESETn	I	low	Asynchronous host reset
PCLK	I	rising	Synchronous host clock
HS_DATA_OUTPUT[15:0]	O	data	Data output
HS_DATA_INPUT[15:0]	I	data	Data input
HS_DATA_WRITE	I	high	Data write
HS_DATA_READ	I	high	Data read
HS_RDY	I	high	Data ready
HS_ACK	O	high	Data acknowledge
HS_ERR	O	high	Data error
HS_BUSY	O	high	Data busy

Pin name	Direction	Active	Description
HS_debug_mode	I	high	Debug mode input
LP_OVF_event	O	high	Overflow event
LP_COMPARE_MATCH_event	O	high	Compare match event
LP_WKUP0_event	O	high	WKUP0 event
LP_TIMESTAMP_CAPTURED_event	O	high	Timestamp captured event
LP_WAKE_UP	O	high	Host wake-up
LP_clock_request	O	high	Clock request
ram_clk	O	rising	Ram cock
ram_clk_en	O	high	Ram clock enable
ram_cs	O	high	Ram chip select
ram_we	O	high	Ram write enable
ram_addr[ram_width-1:0]	O	data	Ram address
ram_din[31:0]	I	data	Ram data input
ram_dout[31:0]	O	data	Ram data output
WKUP0	I	conf.	WKUP0 input
SHDN	O	conf.	SHDN output
SHDN_oe	O	high	SHDN output enable

Table 3. CC-APB_RTC Generic Parameters.

Generic name	Type	Range	Description
RTC_width	integer	1:32	RTC timer counter width
prescaler_width	integer	1:32	Prescaler counter width
debounce_counter_width	integer	1:32	Debounce counter width
default_interrupt_MAPPING	integer	1:32767	Reset value of interrupt_MAPPING register
ram_en	integer	0:1	Backup RAM enable
ram_width	integer	1:10	Backup RAM address width

Table 4. CC-LP_RTC Generic Parameters.

Generic name	Type	Range	Description
RTC_width	integer	1:32	RTC timer counter width
prescaler_width	integer	1:32	Prescaler counter width
debounce_counter_width	integer	1:32	Debounce counter width
ram_en	integer	0:1	Backup RAM enable
ram_width	integer	1:10	Backup RAM address width

Table 5. Resource utilization.

Module	Configuration	ASIC Gates [kGE]
CC-APB_RTC	typical	4.3
CC-LP_RTC	typical	3.7