PERIPHERAL DIRECT MEMORY ACCESS CONTROLLER

Name	Description	
CC-PDMA-APB-AHB	Peripheral Direct Memory Access Controller with APB and AHB-Lite Interface	
Category	**Type**	**Status**
MCU Peripherals	DMA	Silicon and FPGA Proven

Deliverables

- Unencrypted RTL code
- User manual
- Testbench
- C header file
- Support

Features

- AMBA APB3 slave bus
- AMBA AHB-Lite master bus
- Configurable number of peripheral channels
- 8, 16, 32 bits data transfer modes
- Upstream and downstream data aggregation to 32 bit chunks
- Various address modes
- Various arbiter priority schemes
- Configurable independent upstream and downstream FIFOs
- Circular buffer support
- Maskable interrupts
- Dedicated upstream and downstream peripherals DMA interface
- Fully synthesizable synchronous design with positive edge clocking
- DFT ready
- Technology independent IP Core
- Flexible licensing scheme

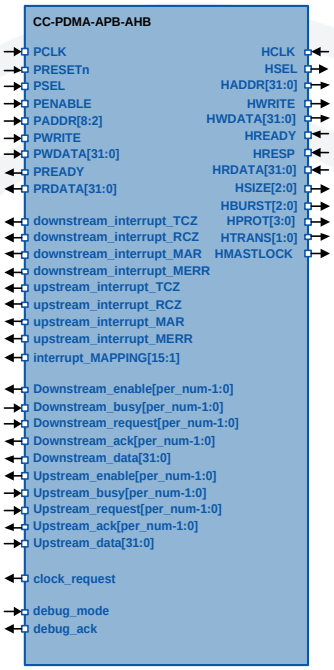
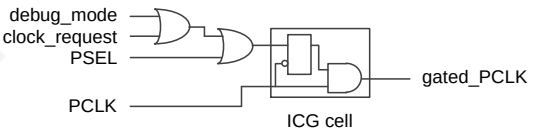
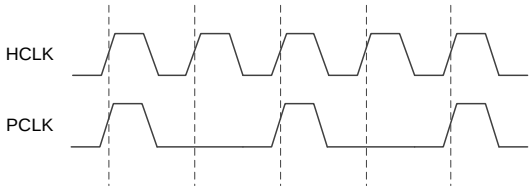


Figure 1. Symbol.



a) Using clock_request pin for low power mode



b) Using different clock ratio for AMBA AHB and APB buses

Figure 2. Integration example.

ChipCraft Sp. z o.o.
Bukowinska 22 lok. 9B
02-703 Warsaw, POLAND

www.chipcraft-ic.com

Table 1. Pin description.

Pin name	Direction	Active	Description
Global signals			
PCLK	I	rising	Synchronous APB clock
PRESETn	I	low	Asynchronous reset
AMBA APB slave signals			
PSEL	I	high	APB peripheral select
PENABLE	I	high	APB bus enable
PADDR[reg_ADDR_width+1:2]	I	data	APB bus address
PWRITE	I	high	APB bus write
PWDATA[31:0]	I	data	APB bus write data
PREADY	O	high	APB bus ready
PRDATA[31:0]	O	data	APB bus read data
Interrupt signals			
downstream_interrupt_TCZ	O	high	Transfer counter zero interrupt
downstreaminterrupt_RCZ	O	high	Reload counter zero interrupt
downstreaminterrupt_MAR	O	high	Memory address reloaded interrupt
downstreaminterrupt_MERR	O	high	Memory access error interrupt
upstream_interrupt_TCZ	O	high	Transfer counter zero interrupt
upstreaminterrupt_RCZ	O	high	Reload counter zero interrupt
upstreaminterrupt_MAR	O	high	Memory address reloaded interrupt
upstreaminterrupt_MERR	O	high	Memory access error interrupt
interrupt_MAPPING[15:1]	O	data	Interrupt mapping vector
Downstream_enable [peripherals_numer-1:0]	O	high	PDMA downstream enable signal
PDMA signals			
Downstream_busy [peripherals_numer-1:0]	I	high	PDMA downstream busy signal
Downstram_request [peripherals_numer-1:0]	I	high	PDMA downstream request signal
Downstream_ack [peripherals_numer-1:0]	O	high	PDMA downstream acknowledge signal
Downstream_data[31:0]	O	data	PDMA downstream data
Upstream_enable [peripherals_numer-1:0]	O	high	PDMA upstream enable signal
Upstream_busy [peripherals_numer-1:0]	I	high	PDMA upstream busy signal
Upstram_request [peripherals_numer-1:0]	I	high	PDMA uptream request signal
Upstream_ack [peripherals_numer-1:0]	O	high	PDMA upstream acknowledge signal
Upstream_data[31:0]	I	data	PDMA upstream data
Debug and power management signals			
clock_request	O	high	Clock request signal
debug_mode	I	high	Debug mode input
debug_ack	O	high	Debug mode acknowledge

Pin name	Direction	Active	Description
AMBA AHB-lite master signals			
HCLK	I	rising	Synchronous AHB clock
HSEL	O	high	AHB peripheral select
HADDR[31:0]	O	data	AHB bus address
HWRITE	O	high	AHB bus write
HWDATA[31:0]	O	data	AHB bus write data
HREADY	I	high	AHB bus ready
HRESP	I	data	AHB bus response
HRDATA[31:0]	I	data	AHB bus read data
HSIZE[2:0]	O	data	AHB bus transfer size
HBURST[2:0]	O	data	AHB bus transfer burst
HPROT[3:0]	O	data	AHB bus transfer protection control
HTRANS[1:0]	O	data	AHB bus transfer type
HMASTLOCK	O	high	AHB bus locked transfer

Table 2. Generic Parameters.

Generic name	Type	Range	Description
reg_ADDR_width	integer	1:32	APB PADDR signal width
peripherals_numer	integer	1:32	Configure number of peripherals
peripheral_select_width	integer	1:5	Width of the peripheral select register
downstream_channel_number	integer	1:32	Number of downstream channels
downstream_channel_number _width	integer	1:5	Downstream channels number width
upstream_channel_number	integer	1:32	Number of upstream channels
upstream_channel_number_width	integer	1:5	Upstream channels number width
downstream_data_aggregation _and_FIFO_enable	integer	0, 1	Enable downstream data aggregation
downstream_fifo_depth	integer	0:32	Downstream FIFO depth
downstream_fifo_depth_width	integer	0:5	Downstream FIFO depth width
upstream_data_aggregarion_enable	integer	0, 1	Enable upstream data aggregation
upstream_fifo_depth	integer	0:32	Upstream FIFO depth
upstream_fifo_depth_width	integer	0:5	Upstream FIFO depth width
upstream_fifo_water_level	integer	0:32	Water level of upstream FIFO
default_interrupt_MAPPING	integer	0:32767	Reset value of interrupt_MAPPING register
LOAD_DELAY	integer	0, 1	Additional register DMA channel output data
AHB_HPROT	integer	0:15	The value passed to the AHB HPROT output
BIG_ENDIAN	integer	0, 1	Endianness of AHB-Lite port