I2C MASTER CONTROLLER

Name	Description	
CC-I2C_MST-APB	I2C Master Controller with APB Interface	
Category	**Type**	**Status**
Serial/Parallel Interfaces	I2C	Silicon and FPGA Proven

Deliverables

- Unencrypted RTL code
- User manual
- Testbench
- C header file
- Support

Features

- I2C-compatible interface
- AMBA APB3 bus
- Standard and custom data rates
- Configurable setup/hold times
- Multi-master support
- Clock stretching support
- Programmable SDA/SCL input filter
- Automatic Start, Stop, Repeated Start, Acknowledge support
- 7 and 10 bit addressing format support Maskable interrupts
- Dedicated upstream and downstream
- DMA interface
- Fully synthesizable synchronous design with positive edge clocking
- DFT ready
- Technology independent IP Core
- Flexible licensing scheme

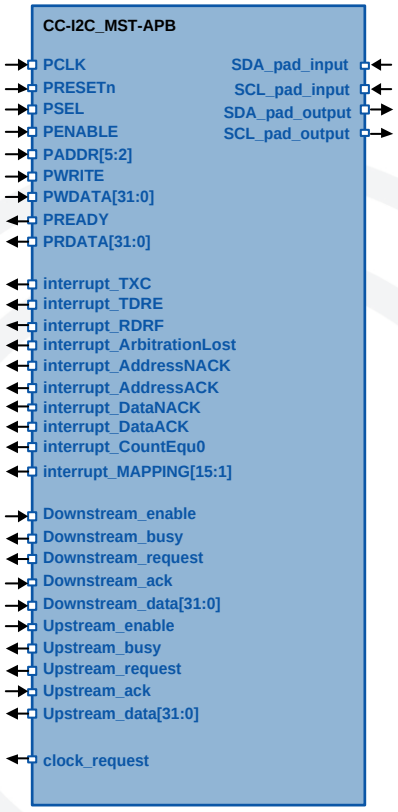
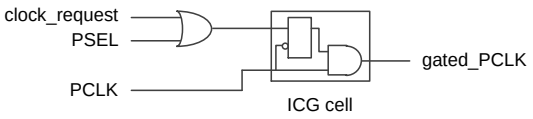
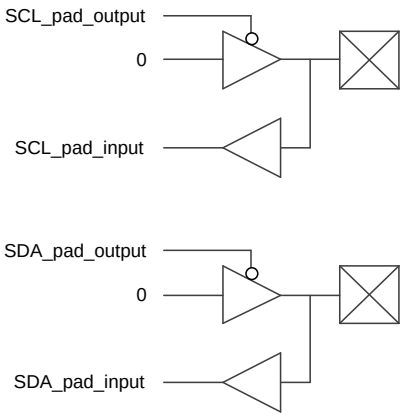


Figure 1. Symbol.



a) Using clock_request pin for low power mode



b) Pad connection example

Figure 2. Integration example.

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Table 1. Pin description.

Pin name	Direction	Active	Description
PCLK	I	rising	Synchronous clock
PRESETn	I	low	Asynchronous reset
PSEL	I	high	APB peripheral select
PENABLE	I	high	APB bus enable
PADDR[5:2]	I	data	APB bus address
PWRITE	I	high	APB bus write
PWDATA[31:0]	I	data	APB bus write data
PREADY	O	high	APB bus ready
PRDATA[31:0]	O	data	APB bus read data
interrupt_TXC	O	high	Transmission complete interrupt
interrupt_TDRE	O	high	Transmit data register empty interrupt
interrupt_RDRF	O	high	Read data register full interrupt
interrupt_ArbitrationLost	O	high	Arbitration lost interrupt
interrupt_AddressNACK	O	high	Address NACK interrupt
interrupt_AddressACK	O	high	Address ACK interrupt
interrupt_DataNACK	O	high	Data NACK interrupt
interrupt_dataACK	O	high	Data ACK interrupt
Interrupt_CountEqu0	O	high	Count equals zero interrupt
interrupt_MAPPING[15:1]	O	data	Interrupt mapping vector
Downstream_enable	I	high	PDMA downstream enable signal
Downstream_busy	O	high	PDMA downstream busy signal
Downstram_request	O	high	PDMA downstream request signal
Downstream_ack	I	high	PDMA downstream ack signal
Downstream_data[31:0]	I	data	PDMA downstream data
Upstream_enable	I	high	PDMA upstream enable signal
Upstream_busy	O	high	PDMA upstream busy signal
Upstram_request	O	high	PDMA upstream request signal
Upstream_ack	I	high	PDMA upstream ack signal
Upstream_data[31:0]	O	data	PDMA upstream data
clock_request	O	high	Clock request signal
SDA_pad_input	I	As I2C spec.	I2C data pin input
SCL_pad_input	I	As I2C spec.	I2C clock pin input
SDA_pad_output	O	As I2C spec.	I2C data pin output
SCL_pad_output	O	As I2C spec.	I2C clock pin output

Table 2. Generic Parameters.

Generic name	Type	Range	Description
PDMA_support	integer	0, 1	Configure PDMA interface support
i2cPrescalerWidth	integer	1:32	Configure clock prescaler width
i2cCountWidth	integer	1:32	Configure data counter width
default_interrupt_MAPPING	integer	0:32767	Reset value of interrupt_MAPPING register

Table 3. Resource utilization.

Configuration	ASIC Gates [kGE]
typical	4