GENERAL PURPOSE INPUT/OUTPUT CONTROLLER

Name	Description	
CC-GPIO-APB	General Purpose Input/Output Controller with APB Interface	
Category	**Type**	**Status**
Serial/Parallel Interfaces	GPIO	Silicon and FPGA Proven
Deliverables		
♦ Unencrypted RTL code ♦ User manual ♦ Testbench	♦ C header file ♦ Support	
Features		
♦ AMBA APB3 bus ♦ Individual configuration of each GPIO pin ♦ Dynamic programming of each GPIO pin as input or output ♦ Configurable level or edge triggered interrupts	♦ Alternative functions support ♦ Fully synthesizable synchronous design with positive edge clocking ♦ DFT ready ♦ Technology independent IP Core ♦ Flexible licensing scheme	

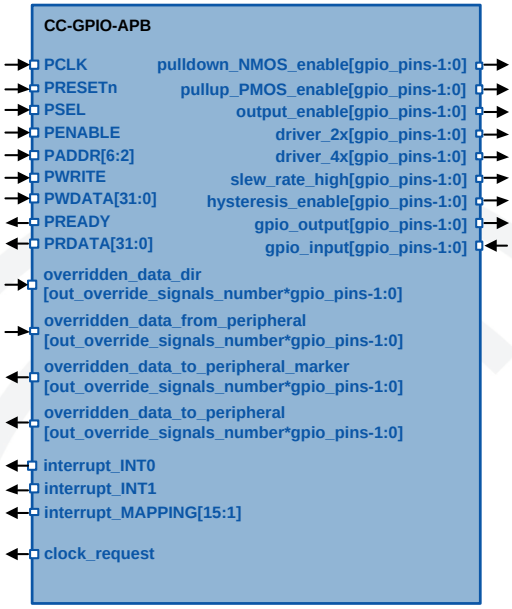
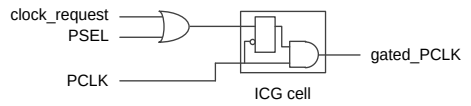
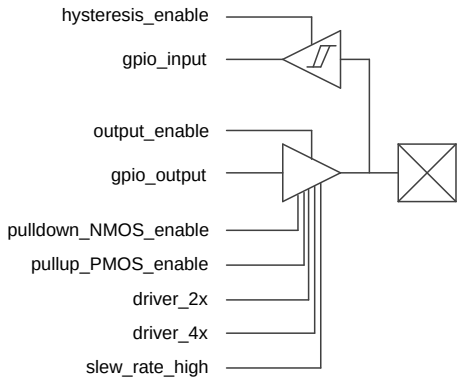


Figure 1. Symbol.



a) using clock_request pin for low power mode



b) pad connection example

Figure 2. Integration example.

ChipCraft Sp. z o.o.
Bukowinska 22 lok. 9B
02-703 Warsaw, POLAND

www.chipcraft-ic.com

Table 1. Pin description.

Pin name	Direction	Active	Description
PCLK	I	rising	Synchronous clock
PRESETn	I	low	Asynchronous reset
PSEL	I	high	APB peripheral select
PENABLE	I	high	APB bus enable
PADDR[6:2]	I	data	APB bus address
PWRITE	I	high	APB bus write
PWDATA[31:0]	I	data	APB bus write data
PREADY	O	high	APB bus ready
PRDATA[31:0]	O	data	APB bus read data
pulldown_NMOS_enable[gpio_pins-1:0]	O	high	Pull down enable signal
pullup_PMOS_enable[gpio_pins-1:0]	O	high	Pull up enable signal
output_enable[gpio_pins-1:0]	O	high	Output enable signal
driver_2x[gpio_pins-1:0]	O	high	Driver 2x selection signal
driver_4x[gpio_pins-1:0]	O	high	Driver 4x selection signal
slew_rate_high[gpio_pins-1:0]	O	high	High slew rate enable signal
hysteresis_enable[gpio_pins-1:0]	O	high	Hysteresis enable signal
gpio_output[gpio_pins-1:0]	O	data	Driver output signal
gpio_input[gpio_pins-1:0]	I	data	Pad input signal
overridden_data_dir [out_override_signals_number *gpio_pins-1:0]	I	high	Alternative functions direction signal
overridden_data_from_peripheral [out_override_signals_number *gpio_pins-1:0]	I	data	Alternative functions data from peripherals
overridden_data_to_peripheral_marker [out_override_signals_number *gpio_pins-1:0]	O	high	Alternative functions selection marker
overridden_data_to_peripheral [gpio_pins-1:0]	O	data	Alternative functions data to peripherals
interrupt_INT0	O	high	INT0 interrupt line
interrupt_INT1	O	high	INT1 interrupt line
interrupt_MAPPING[15:1]	O	data	Interrupt mapping vector
clock_request	O	high	Clock request signal

Table 2. Generic Parameters.

Generic name	Type	Range	Description
gpio_pins	integer	1:32	Number of GPIO pins
out_override_signals_number	integer	0, 1, 3	Number of GPIO alternative functions
out_override_select_width	integer	0, 1, 2	Width of alternative functions select register
default_interrupt_MAPPING	integer	0:32767	Reset value of interrupt_MAPPING register