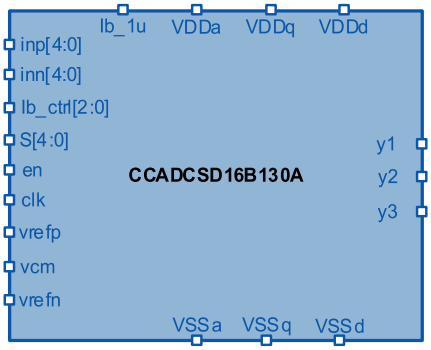
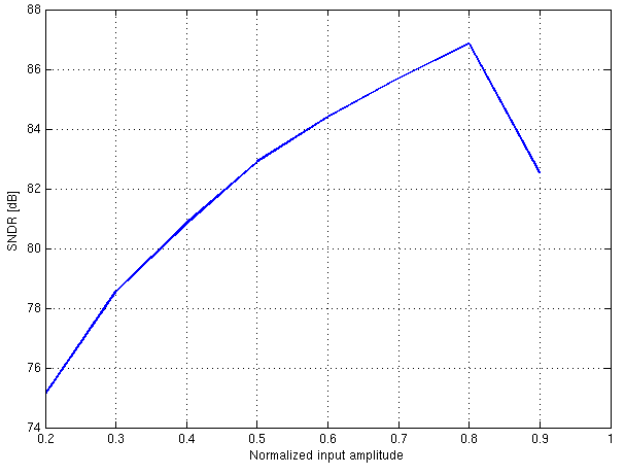
CCADCSD16B130A - 16-bit Sigma-Delta Analog-to-Digital Converter (UMC 130nm)

Symbol



Pin list

Pin	Description	IO	Type
inp[4:0]	Positive input voltages	I	Analog
inn[4:0]	Negative input voltages	I	Analog
Ib_1u	Bias current input (1µA)	I	Analog
vrefp	Positive voltage reference (0.9V)	I	Analog
vrefn	Negative voltage reference (0.3V)	I	Analog
vcm	Comm. mode voltage ref. (0.6 V)	I	Analog
y1	Second order output	O	Digital
y2	Third order output	O	Digital
y3	Fourth order output	O	Digital
Ib_ctrl[2:0]	Bias current control	I	Digital
S[4:0]	Input signal select	I	Digital
en	Enable	I	Digital
clk	Clock (2 MHz)	I	Digital
VDDa	Analog supply (1.2 V)	IO	Supply
VDDa	Mixed signal supply (1.2 V)	IO	Supply
VDDa	Digital supply (1.2 V)	IO	Supply
VSSa	Analog ground	IO	Supply
VSSq	Mixed signal ground	IO	Supply
VSSd	Digital ground	IO	Supply



SNDR vs normalized input amplitude

Product Overview

The cell is a silicon proven 16-bit Sigma-Delta using MASH 2-1-1 architecture. The ADC achieves 86.5 dB SNDR (14 bit ENOB) with Oversampling Ratio OSR equal to 64.

Key Features and Parameters

- Foundry, Node: UMC 130 nm LL/FSG
- Area: 0.21 mm^2, size: 700 µm x 300 µm
- Supply Voltage: 1.08 V ÷ 1.32 V
- Operational Temp. Range: −40°C ÷ 125°C
- I_{DD} < 180 µA
- Clock frequency up to 2 MHz
- 86.5 dB SNDR with 64 OSR (4-stage CIC decimation filter)
- 14 ENOB with 64 OSR (4-stage CIC decimation filter)
- Power consumption to sampling speed trade-off thanks to 3 bit bias current control
- Five multiplexed inputs
- Noise Cancelation Logic, Decimator and Controller with PDMA interface available

Applications

- Sensors
- ECG, EMG, EEG measurement front ends

Deliverables

- Datasheet/Integration Guide
- GDSII database/LVS & SPICE netlist
- HDL Model/Footprint (.LEF)
- IP implement. support, 6 months maintenance (delivery of the IP and documentation up-dates)

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