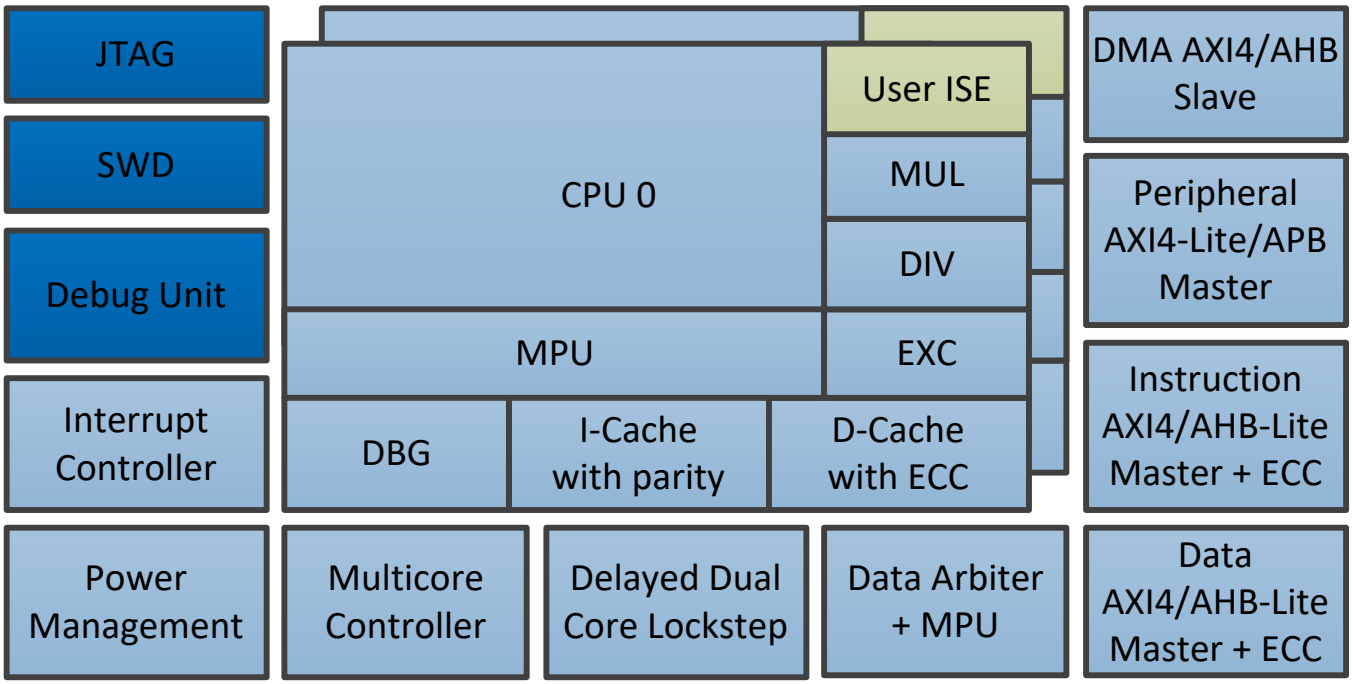
32-bit High Reliability CC200-C Processor Core

Features

- High Performance 32-bit RISC CPU
- Proprietary 6-stage pipeline
- Based on MIPS®-II* instruction set
- Variable delayed dual-core lockstep operation
- Split dual-core mode for high-performance operation
- Up to 1.37 DMIPS/MHz/Core
- Up to 2.29 CoreMark/MHz/Core
- Custom instruction set extension
- Set-associative caches with data snooping and parity
- Power-down mode
- On-chip debug support
- Separate or joint Instruction/Data interface with ECC
- JTAG and 2-pin Serial Wire Debug
- Free GNU-Based C/GDB toolchain
- Cycle accurate simulator
- Synthesizable RTL Verilog source code



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