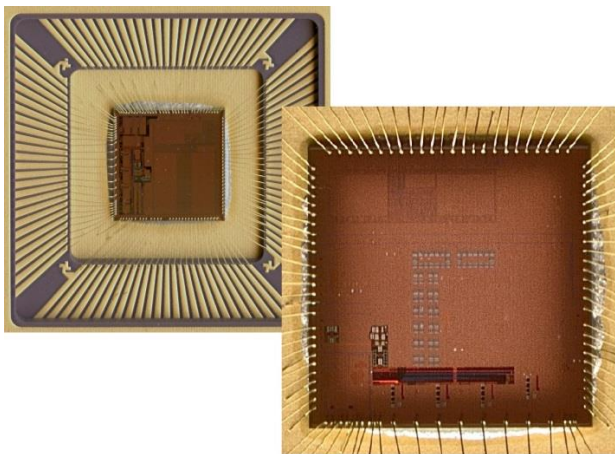
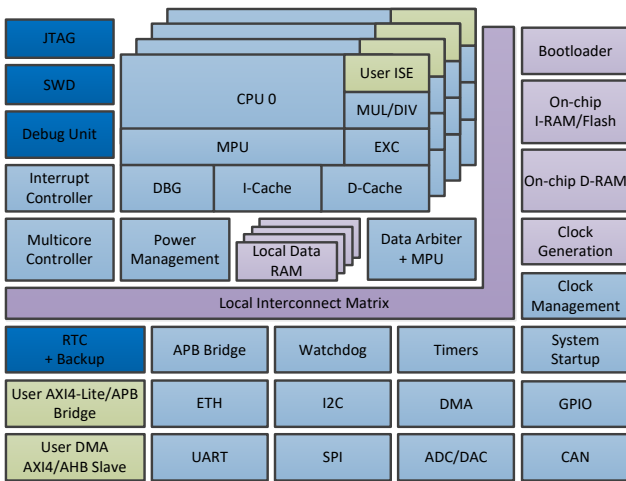
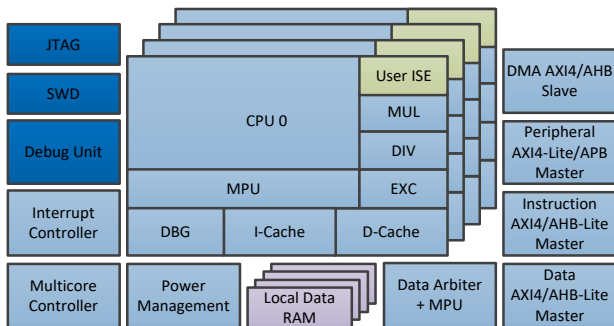


32-bit High Performance CC100 Processor/Microcontroller IP



Features

- High Performance CC100-C Processor Core
- High Performance CC100-S System-on-Chip
- Proprietary 6-stage pipeline
- Based on MIPS[®]-II* instruction set
- Single or multicore implementation
- Up to 1.37 DMIPS/MHz/Core
- Up to 2.29 CoreMark/MHz/Core
- Optional set-associative caches with data snooping
- Power-down mode
- On-chip debug support
- FPGA and silicon proven
- JTAG or 2-pin Serial Wire Debug

Benefits

- Synthesizable RTL Verilog source code
- Cycle accurate simulator
- Custom instruction set extension
- Mature free GNU-Based C/GDB toolchain
- Full implementation and maintenance support with individual approach
- Low-cost and flexible licensing
- Embedded solution for low-power and low-footprint applications
- Suitable for mobile, IoT and wearable devices

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