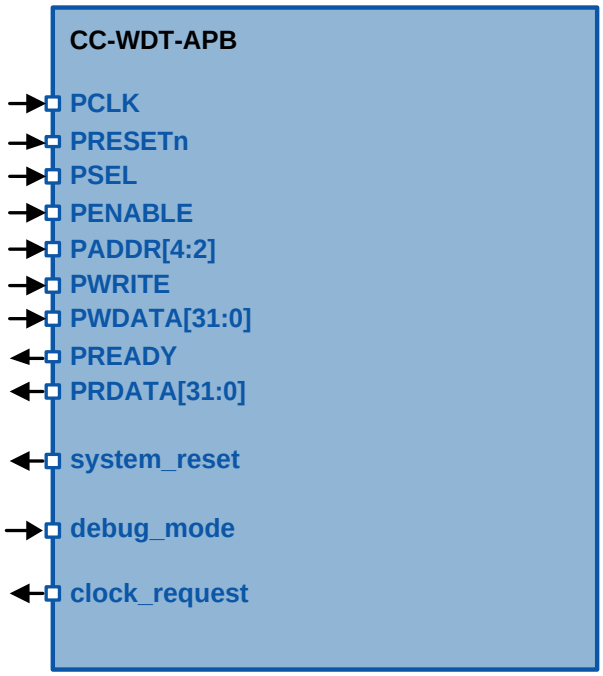
CC-WDT-APB Configurable Watchdog Timer

Symbol



Features

- AMBA APB3 bus
- Configurable timeout interval
- Standard and windowed mode
- Stop in debug mode option
- Register write protection
- Fully synthesizable synchronous design with positive edge clocking
- DFT ready

Benefits

- Supplied as human-readable Verilog RTL source code
- Technology independent IP Core
- Suitable for FPGA and ASIC
- Silicon and FPGA proven
- Easy SoC integration
- Full implementation and maintenance support with individual approach
- Flexible licensing scheme

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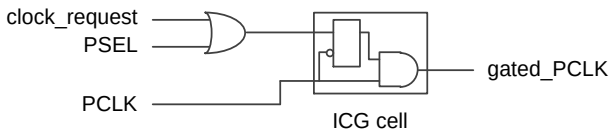
Generic Parameters

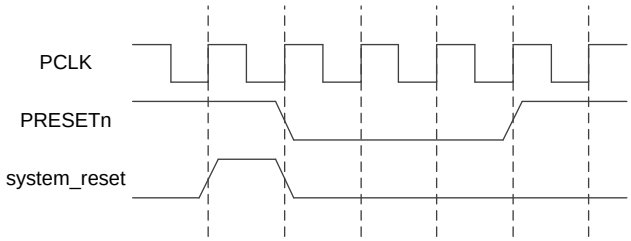
Generic name	Description	Type	Range
watchdog_width	Watchdog timer width	integer	1:32
prescaler_width	Watchdog timer prescaler width	integer	1:32

Integration example

- Using clock_request pin for low power mode:



- Timing of reset synchronizer connected to system_reset pin:



Pin-out Description

Pin name	Description	I/O	Active
PCLK	Synchronous clock	I	rising
PRESETn	Asynchronous reset	I	low
PSEL	APB peripheral select	I	high
PENABLE	APB bus enable	I	high
PADDR[4:2]	APB bus address	I	data
PWRITE	APB bus write	I	high
PWDATA[31:0]	APB bus write data	I	data
PREADY	APB bus ready	O	high
PRDATA[31:0]	APB bus read data	O	data
system_reset	Watchdog system reset output	O	high
debug_mode	Debug mode input	I	high
clock_request	Clock request signal	O	high