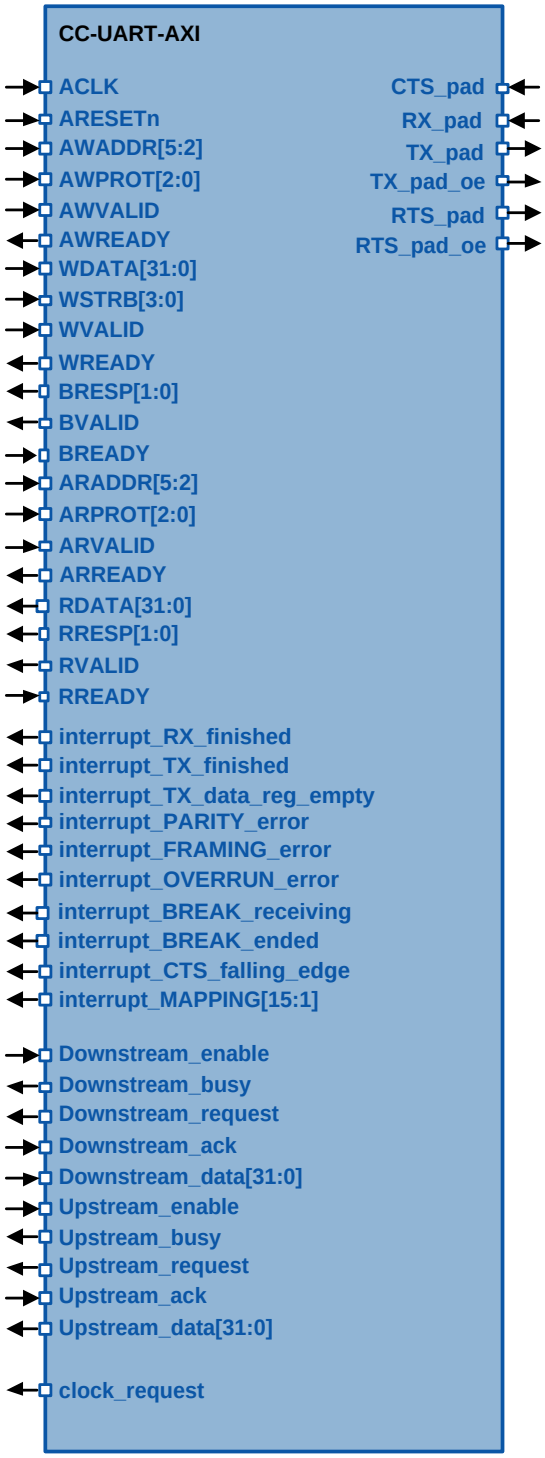
CC-UART-AXI UART Serial Interface Controller

Symbol



Features

- UART-compatible interface
- AMBA AXI4-Lite bus
- Full duplex
- Custom baud rate generation
- 8x, 16x oversampling
- 5, 6, 7, 8, 9 bits data
- 1, 2 stop bits
- LSB or MSB mode
- Configurable parity
- Hardware flow control
- RS485 mode
- Maskable interrupts
- Dedicated upstream and downstream DMA interface
- Fully synthesizable synchronous design with positive edge clocking
- DFT ready

Benefits

- Supplied as human-readable Verilog RTL source code
- Technology independent IP Core
- Suitable for FPGA and ASIC
- Silicon and FPGA proven
- Easy SoC integration
- Full implementation and maintenance support with individual approach
- Flexible licensing scheme

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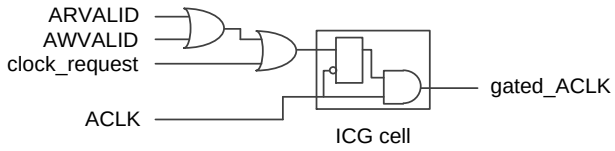
Generic Parameters

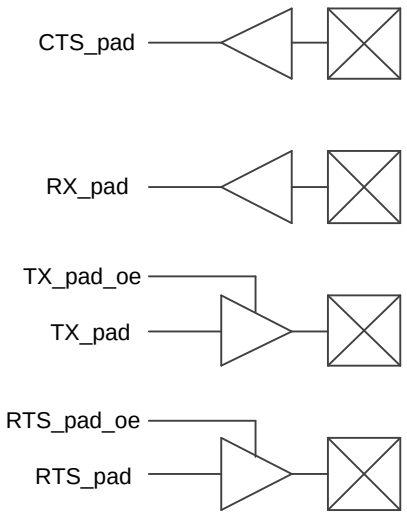
Generic name	Description	Type	Range
PDMA_support	Configure PDMA interface support	integer	0, 1
default_interrupt _MAPPING	Reset value of interrupt_MAPPING register	integer	0:32767

Integration example

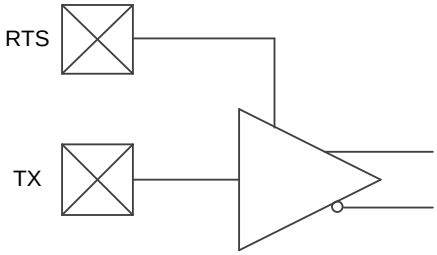
- Using clock_request pin for low power mode:



- Pad connection example:



- RS485 mode:



Pin-out Description

Pin name	Description	I/O	Active
ACLK	Synchronous clock	I	rising
ARESETn	Asynchronous reset	I	low
AWADDR[5:2]	AXI write address	I	data
AWPROT[2:0]	AXI write address protection type	I	data
AWVALID	AXI write address valid	I	high
AWREADY	AXI write address ready	O	high
WDATA[31:0]	AXI write data	I	data
WSTRB[3:0]	AXI write strobe	I	high
WVALID	AXI write valid	I	high
WREADY	AXI write ready	O	high
BRESP[1:0]	AXI write response	O	data
BVALID	AXI write response valid	O	high
BREADY	AXI write response ready	I	high
ARADDR[5:2]	AXI read address	I	data
ARPROT[2:0]	AXI read address protection type	I	data
ARVALID	AXI read address valid	I	High
ARREADY	AXI read address ready	O	high
RDATA[31:0]	AXI read data	O	data
RRESP[1:0]	AXI read response	O	data
RVALID	AXI read valid	O	high
RREADY	AXI read ready	I	high
interrupt_RX_finished	Reception finished interrupt	O	high
interrupt_TX_finished	Transmission finished interrupt	O	high
interrupt_TX_data_reg _empty	Transmit data register empty interrupt	O	high
interrupt_PARITY_error	Parity error interrupt	O	high
interrupt_FRAMING_error	Framing error interrupt	O	high
interrupt_OVERRUN _error	Overrun error interrupt	O	high
interrupt_BREAK _receiving	Break receiving interrupt	O	High
interrupt_BREAK _ending	Break ended interrupt	O	high
interrupt_CTS_falling _edge	CTS falling edge interrupt	O	high
interrupt_MAPPING[15:1]	Interrupt mapping vector	O	data
Downstream_enable	PDMA downstream enable	I	high
Downstream_busy	PDMA downstream busy	O	high
Downstram_request	PDMA downstream request	O	high
Downstream_ack	PDMA downstream ack	I	high
Downstream_data[31:0]	PDMA downstream data	I	data
Upstream_enable	PDMA upstream enable	I	high
Upstream_busy	PDMA upstream busy	O	high
Upstram_request	PDMA uptream request	O	high
Upstream_ack	PDMA upstream ack	I	high
Upstream_data[31:0]	PDMA upstream data	O	data

clock_request	Clock request signal	O	high
CTS_pad	UART Clear To Send	I	low
RX_pad	UART Reveive Input	I	data
TX_pad	UART Transmit Output	O	data
TX_pad_oe	UART TX output enable	O	high
RTS_pad	UART Ready To Send	O	low/high
RTS_pad_oe	UART RTS output enable	O	high