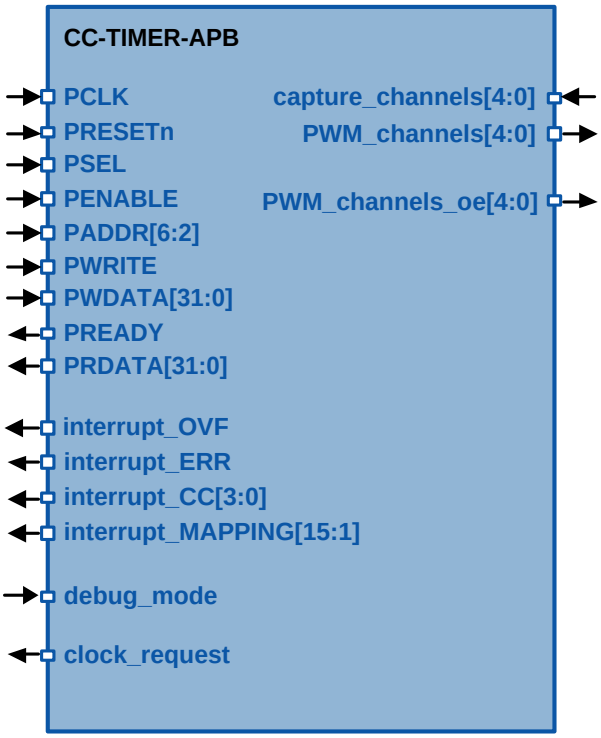
CC-TIMER-APB Configurable Timer Counter

Symbol



Features

- AMBA APB3 bus
- Programmable multi-function timer
- Double buffered configuration registers
- Configurable single/dual slope PWM outputs
- Configurable standard/period/pulse input capture mode
- Stop in debug mode option
- Fully synthesizable synchronous design with positive edge clocking
- DFT ready

Benefits

- Supplied as human-readable Verilog RTL source code
- Technology independent IP Core
- Suitable for FPGA and ASIC
- Silicon and FPGA proven
- Easy SoC integration
- Full implementation and maintenance support with individual approach
- Flexible licensing scheme

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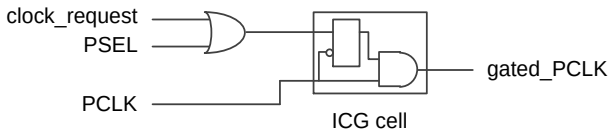
Generic Parameters

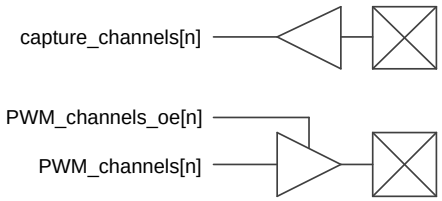
Generic name	Description	Type	Range
timer_width	Timer counter width	integer	1:32
prescaler_width	Timer prescaler width	integer	1:32
address_width	APB PADDR signal width	integer	1:32
cc_channels _number	Number of capture/compare channels	integer	0:4
default_interrupt _MAPPING	Reset value of interrupt_MAPPING register	integer	0:32767

Integration example

- Using clock_request pin for low power mode:



- Pad connection example:



Pin-out Description

Pin name	Description	I/O	Active
PCLK	Synchronous clock	I	rising
PRESETn	Asynchronous reset	I	low
PSEL	APB peripheral select	I	high
PENABLE	APB bus enable	I	high
PADDR [address_width+1:2]	APB bus address	I	data
PWRITE	APB bus write	I	high
PWDATA[31:0]	APB bus write data	I	data
PREADY	APB bus ready	O	high
PRDATA[31:0]	APB bus read data	O	data
capture_channels [cc_channels_number:0]	Timer capture inputs	I	data
PWM_channels [cc_channels_number:0]	Timer PWM outputs	O	data
PWM_channels_oe [cc_channels_number:0]	Timer PWM output enable	O	high
interrupt_OVF	Timer overflow interrupt	O	high
interrupt_ERR	Capture mode error interrupt	O	high
interrupt_CC [cc_channels_number:0]	Capture/compare interrupt	O	high
interrupt_MAPPING[15:1]	Interrupt mapping vector	O	data
debug_mode	Debug mode input	I	high
clock_request	Clock request signal	O	high