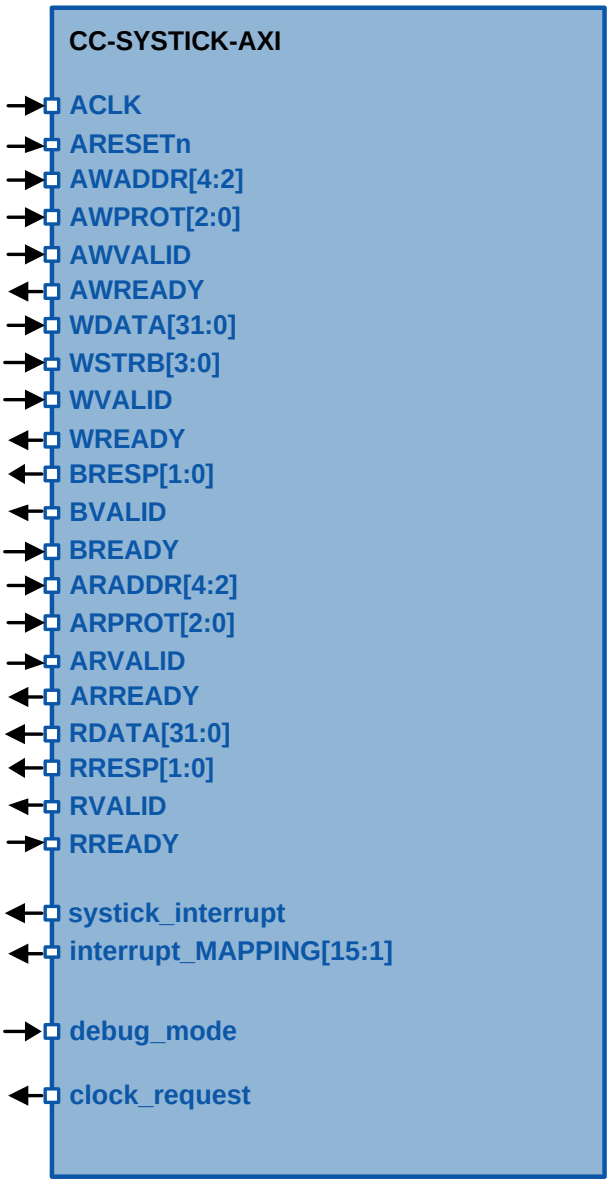
CC-SYSTICK-AXI Configurable System Tick Timer

Symbol



Features

- AMBA AXI4-Lite bus
- Programmable system tick timer
- Configurable prescaler and period
- Configurable interrupts
- Stop in debug mode option
- Fully synthesizable synchronous design with positive edge clocking
- DFT ready

Benefits

- Supplied as human-readable Verilog RTL source code
- Technology independent IP Core
- Suitable for FPGA and ASIC
- Silicon and FPGA proven
- Easy SoC integration
- Full implementation and maintenance support with individual approach
- Flexible licensing scheme

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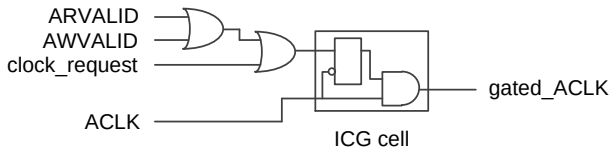
Generic Parameters

Generic name	Description	Type	Range
systick_width	Systick counter width	integer	1:32
prescaler_width	Timer prescaler width	integer	1:32
default_interrupt _MAPPING	Reset value of interrupt_MAPPING register	integer	0:32767

Integration example

- Using clock_request pin for low power mode:



Pin-out Description

Pin name	Description	I/O	Active
ACLK	Synchronous clock	I	rising
ARESETn	Asynchronous reset	I	low
AWADDR[4:2]	AXI write address	I	data
AWPROT[2:0]	AXI write address protection type	I	data
AWVALID	AXI write address valid	I	high
AWREADY	AXI write address ready	O	high
WDATA[31:0]	AXI write data	I	data
WSTRB[3:0]	AXI write strobe	I	high
WVALID	AXI write valid	I	high
WREADY	AXI write ready	O	high
BRESP[1:0]	AXI write response	O	data
BVALID	AXI write response valid	O	high
BREADY	AXI write response ready	I	high
ARADDR[4:2]	AXI read address	I	data
ARPROT[2:0]	AXI read address protection type	I	data
ARVALID	AXI read address valid	I	High
ARREADY	AXI read address ready	O	high
RDATA[31:0]	AXI read data	O	data
RRESP[1:0]	AXI read response	O	data
RVALID	AXI read valid	O	high
RREADY	AXI read ready	I	high
systick_interrupt	Systick interrupt	O	high
interrupt_MAPPING[15:1]	Interrupt mapping vector	O	data
debug_mode	Debug mode input	I	high
clock_request	Clock request signal	O	high