Datasheet

CC-SYSTICK-AXI Documentation

1.1

Scope

This document describes the CC-SYSTICK-AXI IP core. Module features and configuration registers are described. The document contains integration guide that covers synthesis options and instantiation example for easy implementation in customer's environment.

Contents

1. Systick Module

1.1 Functionality

- Incrementing mode,
- overflow interrupt (OVF).

1.2 Overview

Systick module can be used as a interrupt source for tasks that need to be executed regularly. For example allows an OS to carry out context switching to support multiple tasking.

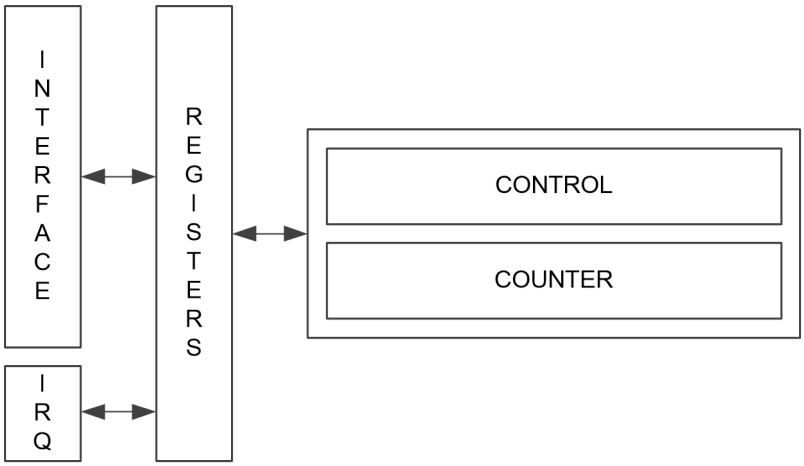


Figure 1.1. Systick block diagram.

Figure 1.1 presents the block diagram of the Systick module. It is composed of configuration registers and main counter register. Prescaler register counts peripheral clock cycles (PCLK) and generates events for main COUNT register (1.4.3). The Systick module has configurable period and works in incrementing mode only.

1.3 Interrupts

The Systick module has one interrupt source.

1.3.1 Systick Interrupt

The Systick Interrupt is signalized by IF flag in IRQF register (1.4.6). Systick interrupt occurs when COUNT (1.4.3) reaches PER value (1.4.4). The interrupt is cleared after reading IRQF register or by writing one in IF bit (1.4.6).

1.4 Configuration Registers

1.4.1 Registers List

The core is controlled through registers mapped into memory address space. Not implemented locations are read as zeros.

Address Offset	Register	Name
0x00	CTRL	Control Register
0x04	COUNT	Count Register
0x08	PER	Period Register
0x0C	PRES	Prescaler Register
0x10	IRQF	Interrupt Flags Register
0x14	IRQMAP	Interrupt Mapping Register

1.4.2 Control Register

Address: 0x00

31	30	...	...	...	...	9	8
DBG_STOP		...	...	...	...		
R/W	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
						IE	EN
R	R	R	R	R	R	R/W	R/W
0	0	0	0	0	0	0	0

EN *Systick Enable*

0 Systick is disabled. Clock to the module is stopped.

1 Systick is enabled. Clock to the module is supplied.

IE *Systick Interrupt Enable*

0 Interrupt disabled.

1 Interrupt enabled.

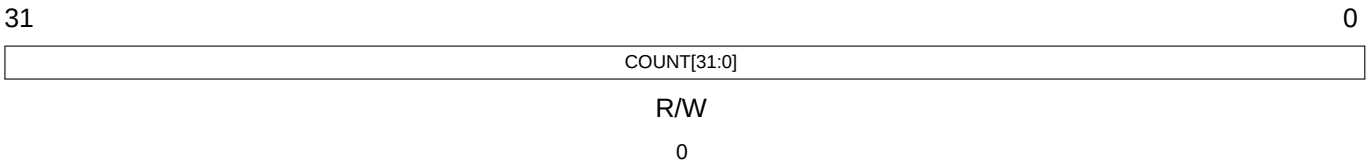
DBG_STOP *Systick stop in debug mode*

0 Systick is counting in debug mode.

1 Systick is not counting in debug mode.

1.4.3 Count Register

Address: 0x04

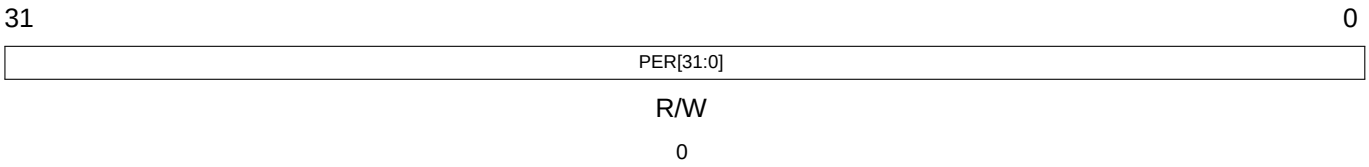


COUNT[31:0] *Current Count*

Current value of Systick counter.

1.4.4 Period Register

Address: 0x08



PER[31:0] *Systick Period*

Systick counter period. Reaching PER value sets interrupt flag (IF, 1.4.6) and clears COUNT register (1.4.3).

1.4.5 Prescaler Register

Address: 0x0C

31	0
PRES[31:0]	
R/W	
0	

PRES[31:0] *Systick Prescaler*

Systick module prescaler. COUNT register (1.4.3) is incremented every each $PRES + 1$ PCLK clock cycles.

1.4.6 Interrupt Flags Register

Address: 0x10

31	30	...	...	...	...	9	8
		...	...	...	...		
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0
7	6	5	4	3	2	1	0
							IF
R	R	R	R	R	R	R	R/W
0	0	0	0	0	0	0	0

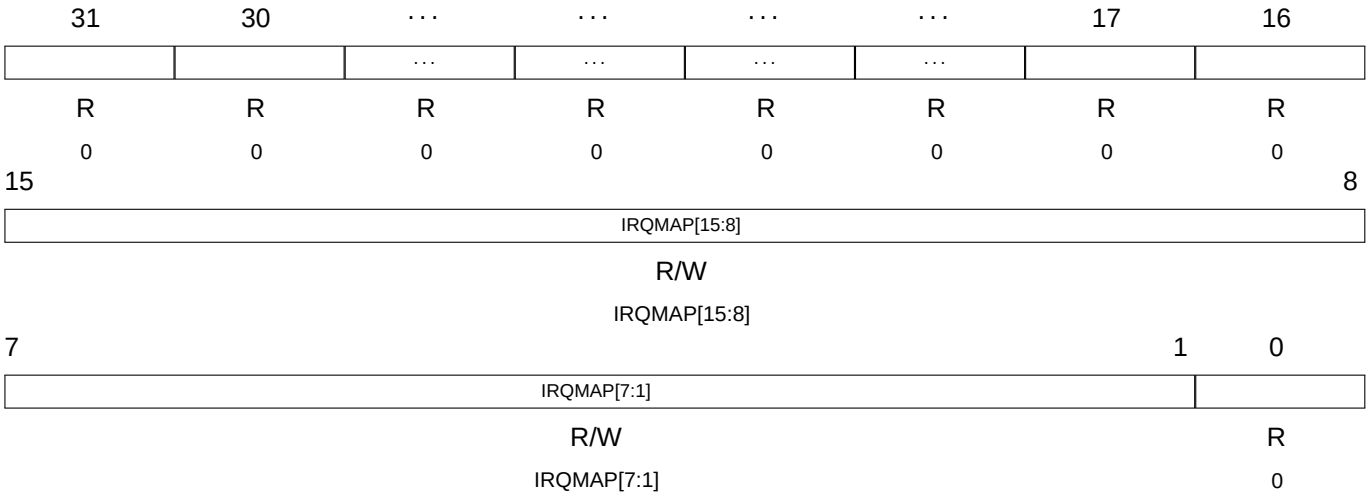
IF *Interrupt Flag*

1 Systick reached PER value.

Bit is cleared after register readout or by writing one to this position.

1.4.7 Interrupt Mapping Register

Address: 0x14



IRQMAP[15:1] *Interrupt Mapping*

Each set bit represents the interrupt number that will be passed to interrupt controller. It is allowed to set more than one bit.

1.5 Implementation

1.5.1 Design Structure

The synthesible RTL IP core part (*AXI/rtl* and *SYSTICK/rtl* folder) utilizes Verilog 2005 HDL. The testbench part (*AXI/tb* and *SYSTICK/tb* folder) uses SystemVerilog language.

```
AXI
├── rtl
│   └── AXI_PERIPH
│       └── amba_axilite_apb_bridge.v
└── tb
    └── AXI_PERIPH
        ├── APB
        │   └── virtual_APB_slave.sv
        ├── AXI
        │   └── tb_amba_axilite_tasks.sv
        ├── common
        │   └── timescale.v
        ├── run
        │   └── ncvlog_amba_axilite_apb_bridge.sh
        ├── tests
        │   └── tb_read_write_test.sv
        └── tb_amba_axilite_apb_bridge.sv
SYSTICK
├── beh
├── rtl
│   ├── APB_SYSTICK.v
│   ├── AXILITE_SYSTICK.v
│   ├── SYSTICK_config.v
│   ├── SYSTICK_defines.v
│   └── SYSTICK.v
└── tb
    ├── APB
    │   ├── tb_APB_SYSTICK_init.v
    │   └── tb_APB_SYSTICK_reg_access_tasks.v
    ├── common
    │   ├── tb_SYSTICK_other_tasks.v
    │   ├── tb_SYSTICK_read_config_tasks.v
    │   ├── tb_SYSTICK_write_config_tasks.v
    │   └── timescale.v
    ├── run
    │   └── ncvlog_apb_systick.sh
    ├── tests
    │   ├── tb_interrupt_MAPPING_test.sv
    │   └── tb_SYSTICK_INCREMENT_test.sv
    └── tb_APB_SYSTICK.sv
└── compile.list
```


1.5.2 Simulation Flow

The IP Core is provided with self-checking testbench to verify the correct operation of the IP prior to use in a design. The testbench is divided into two environments. The first one tests the APB_SYSTICK module. To run the simulation using Cadence® Incisive® Enterprise Simulator run *ncvlog_apb_systick.sh* script located in the *SYSTICK/tb/run* folder. The simulation should end with reporting no errors. The second environment tests the AXI4-Lite to APB3 converter. To run the simulation using Cadence® Incisive® Enterprise Simulator run *ncvlog_amba_axilite_apb_bridge.sh* script located in the *AXI/tb/AXI_PERIPH/run* folder. The simulation should end with reporting no errors. The AXILITE_SYSTICK top module is composed of the APB_SYSTICK core and the amba_axilite_apb_bridge AXI4-Lite to APB3 converter.

1.5.3 Clock and Reset

The CC-SYSTICK-AXI utilizes a fully synchronous design with one positive edge clocking domain and negative asynchronous reset assertion. External reset synchronizer has to be used to ensure synchronous reset deassertion.

1.5.4 Constraints

In most cases only module output ports are registered. Therefore, it is a good practice to reserve the entire clock cycle for module inputs combinational logic and set minimal input delay (*set_input_delay* command). Registered outputs leave the entire clock cycle for external logic (*set_output_delay* command).

1.5.5 Configuration Options

The table below shows the generic parameters of the core.

Generic name	Description	Range	Default
systick_width	Configure width of systick count register	1:32	32
prescaler_width	Configure width of systick prescaler register	1:32	8
default_interrupt_MAPPING	Reset value of interrupt_MAPPING register	0:32767	0

1.5.6 Signals Description

Signal name	Description	I/O	Active	Type
ACLK	Synchronous clock	I	rising	clock
ARESETn	Asynchronous reset	I	low	reset
AWADDR[4:2]	AXI4-Lite write address	I	data	comb.
AWPROT[2:0][1]	AXI4-Lite write address protection type	I	data	comb.
AWVALID	AXI4-Lite write address valid	I	high	comb.
AWREADY	AXI4-Lite write address ready	O	high	reg.
WDATA[31:0]	AXI4-Lite write data	I	data	comb.
WSTRB[3:0]	AXI4-Lite write strobe	I	high	comb.
WVALID	AXI4-Lite write valid	I	high	comb.
WREADY	AXI4-Lite write ready	O	high	reg.
BRESP[1:0]	AXI4-Lite write response	O	data	reg.
BVALID	AXI4-Lite write response valid	O	high	reg.
BREADY	AXI4-Lite write respnse ready	I	high	comb.
ARADDR[4:2]	AXI4-Lite read address	I	data	comb.
ARPROT[2:0][1]	AXI4-Lite read address protection type	I	data	comb.
ARVALID	AXI4-Lite read address valid	I	high	comb.
ARREADY	AXI4-Lite read address ready	O	high	reg.
RDATA[31:0]	AXI4-Lite read data	O	data	reg.
RRESP[1:0]	AXI4-Lite read response	O	data	reg.
RVALID	AXI4-Lite read valid	O	high	reg.
RREADY	AXI4-Lite read ready	I	high	comb.
systick_interrupt	Systick interrupt	O	high	reg.
interrupt_MAPPING[15:1]	Interrupt mapping vector	O	data	reg.
clock_request	Clock request signal	O	high	reg.
debug_mode	Debug mode indicator (1 - core is halted)	I	high	comb.

[1] Signal is not used in the design.

1.5.7 Instantiation

```
icg
icg_stick_u (
    .E(ARVALID|AWVALID|stick_clock_request),
    .clk(ACLK),
    .gclk(stick_clk),
    .scan_enable(scan_enable));

AXILTIE_SYSTICK #(
    .systick_width(CFG_SYSTICK_WIDTH),
    .prescaler_width(CFG_SYSTICK_PRES),
    .default_interrupt_MAPPING(CFG_DEF_INT_MAPPING)
AXILITE_SYSTICK_u (
    .ACLK(stick_clk),
    .ARESETn(ARESETn),
    .AWADDR(AWADDR[4:2]),
    .AWPROT(AWPROT),
    .AWVALID(AWVALID),
    .AWREADY(AWREADY),
    .WDATA(WDATA),
    .WSTRB(WSTRB),
    .WVALID(WVALID),
    .WREADY(WREADY),
    .BRESP(BRESP),
    .BVALID(BVALID),
    .BREADY(BREADY),
    .ARADDR(ARADDR[4:2]),
    .ARPROT(ARPROT),
    .ARVALID(ARVALID),
    .ARREADY(ARREADY),
    .RDATA(RDATA),
    .RRESP(RRESP),
    .RVALID(RVALID),
    .RREADY(RREADY),
    .systick_interrupt(stick_interrupt),
    .interrupt_MAPPING(stick_interrupt_MAPPING),
    .clock_request(stick_clock_request),
    .debug_mode(debug_amba_stall_req));

assign  stick_irq_mapped  = stick_interrupt_MAPPING & {15{stick_interrupt}};
```

1.6 Revision History

Doc. Rev.	Date	Comments
1.1	11-2018	Editorial corrections in 1.5.7 Instantiation section.
1.0	11-2017	First Issue.

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