

CC-SYSTICK-APB Configurable System Tick Timer

Symbol



Features

- AMBA APB3 bus
- Programmable system tick timer
- Configurable prescaler and period
- Configurable interrupts
- Stop in debug mode option
- Fully synthesizable synchronous design with positive edge clocking
- DFT ready

Benefits

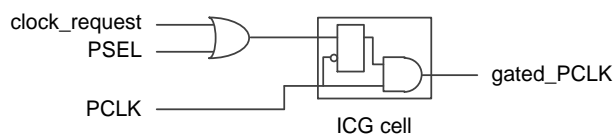
- Supplied as human-readable Verilog RTL source code
- Technology independent IP Core
- Suitable for FPGA and ASIC
- Silicon and FPGA proven
- Easy SoC integration
- Full implementation and maintenance support with individual approach
- Flexible licensing scheme

Generic Parameters

Generic name	Description	Type	Range
systick_width	Systick counter width	integer	1:32
prescaler_width	Timer prescaler width	integer	1:32
default_interrupt_MAPPING	Reset value of interrupt_MAPPING register	integer	0:32767

Integration example

- Using clock_request pin for low power mode:



Pin-out Description

Pin name	Description	I/O	Active
PCLK	Synchronous clock	I	rising
PRESETn	Asynchronous reset	I	low
PSEL	APB peripheral select	I	high
PENABLE	APB bus enable	I	high
PADDR[4:2]	APB bus address	I	data
PWRITE	APB bus write	I	high
PWDATA[31:0]	APB bus write data	I	data
PREADY	APB bus ready	O	high
PRDATA[31:0]	APB bus read data	O	data
systick_interrupt	Systick interrupt	O	high
interrupt_MAPPING[15:1]	Interrupt mapping vector	O	data
debug_mode	Debug mode input	I	high
clock_request	Clock request signal	O	high

