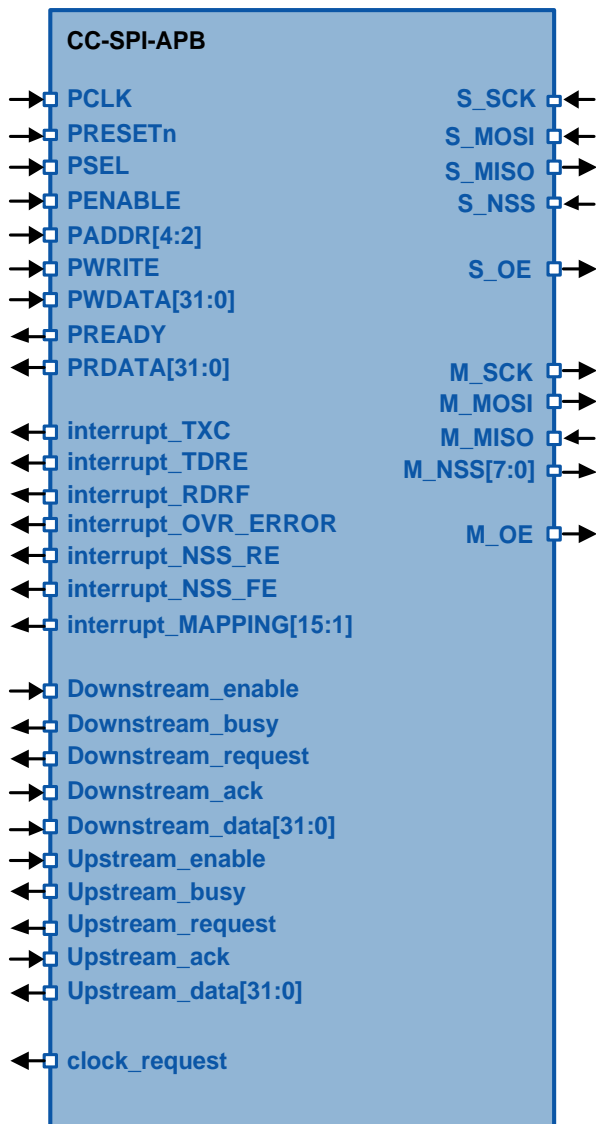


CC-SPI-APB Serial Peripheral Interface Master/Slave

Symbol



Features

- SPI-compatible interface
- AMBA APB3 bus
- Master or slave mode
- Full duplex
- Programmable clock rate up to PCLK/2
- Slave speed up to PCLK/8
- Up to 8 slave select lines
- Slave MISO output enable generation for multiple slaves
- Configurable clock polarity and phase
- LSB or MSB mode
- 8, 16, 24, 32 bits data transfer mode
- Maskable interrupts
- Dedicated upstream and downstream DMA interface
- Fully synthesizable synchronous design with positive edge clocking
- DFT ready

Benefits

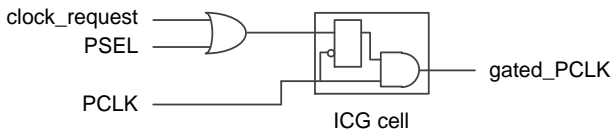
- Supplied as human-readable Verilog RTL source code
- Technology independent IP Core
- Suitable for FPGA and ASIC
- Silicon and FPGA proven
- Easy SoC integration
- Full implementation and maintenance support with individual approach
- Flexible licensing scheme

Generic Parameters

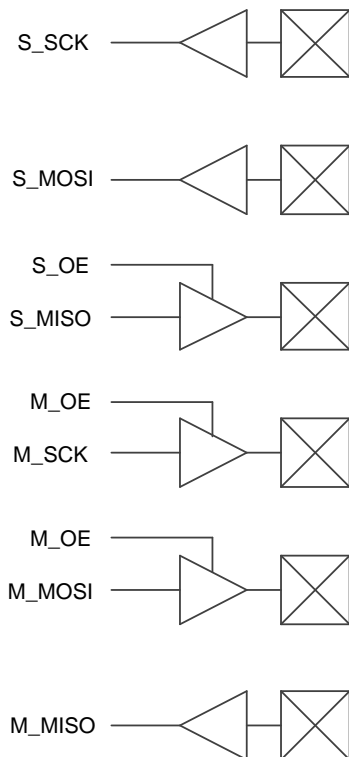
Generic name	Description	Type	Range
PDMA_support	Configure PDMA interface support	integer	0, 1
slave_support	Configure SPI slave support	integer	0,1
default_interrupt_MAPPING	Reset value of interrupt_MAPPING register	integer	0:32767
mss_number	Numer of slave select pins	integer	0:8

Integration example

- Using clock_request pin for low power mode:



- Pad connection example:



Pin-out Description

Pin name	Description	I/O	Active
PCLK	Synchronous clock	I	rising
PRESETn	Asynchronous reset	I	low
PSEL	APB peripheral select	I	high
PENABLE	APB bus enable	I	high
PADDR[4:2]	APB bus address	I	data
PWRITE	APB bus write	I	high
PWDATA[31:0]	APB bus write data	I	data
PREADY	APB bus ready	O	high
PRDATA[31:0]	APB bus read data	O	data
interrupt_TXC	Transmission complete interrupt	O	high
interrupt_TDRE	Transmit data register empty interrupt	O	high
interrupt_RDRF	Read data register full interrupt	O	high
interrupt_OVR_ERROR	Overrun interrupt	O	high
interrupt_NSS_RE	NSS rising edge interrupt	O	high
interrupt_NSS_FE	NSS falling edge interrupt	O	high
interrupt_MAPPING[15:1]	Interrupt mapping vector	O	data
Downstream_enable	PDMA downstream enable signal	I	high
Downstream_busy	PDMA downstream busy signal	O	high
Downstream_request	PDMA downstream request signal	O	high
Downstream_ack	PDMA downstream ack signal	I	high
Downstream_data[31:0]	PDMA downstream data	I	data
Upstream_enable	PDMA upstream enable signal	I	high
Upstream_busy	PDMA upstream busy signal	O	high
Upstream_request	PDMA upstream request signal	O	high
Upstream_ack	PDMA upstream ack signal	I	high
Upstream_data[31:0]	PDMA upstream data	O	data
clock_request	Clock request signal	O	high
S_SCK_pad	SPI Slave clock	I	rising or falling
S_MOSI_pad	SPI Slave Master Out/Slave In	I	data
S_NSS_pad	SPI Slave serial select	I	low
S_MISO_pad	SPI Slave Master In/Slave Out	O	data
S_OE	SPI Slave output enable	O	high
M_MISO_pad	SPI Master Master In/Slave Out	I	data
M_SCK_pad	SPI Master clock	O	rising or falling
M_MOSI_pad	SPI Master Master Out/Slave In	O	data
M_NSS_pad [mss_number:0]	SPI Master serial select	O	low
M_OE	Master output enable	O	high

