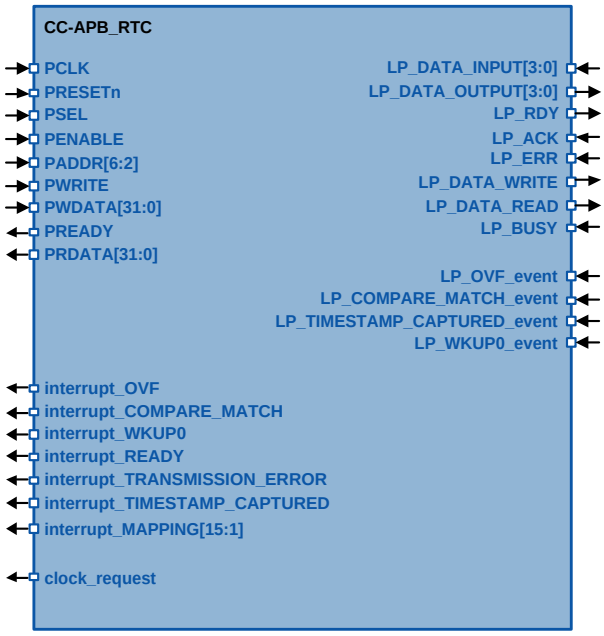
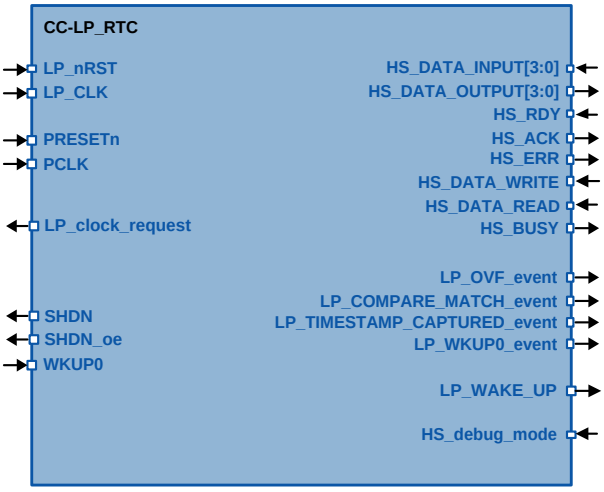
CC-RTC-APB Programmable Real Time Counter

Symbol





Features

- AMBA APB3 bus
- Programmable multi-function RTC timer
- Configurable WKUP0 input
- Configurable SHDN output
- Maskable interrupts
- Timestamp generation
- User backup registers
- Fully synthesizable design with two positive edge clocking clock domains
- DFT ready

Benefits

- Supplied as human-readable Verilog RTL source code
- Technology independent IP Core
- Suitable for FPGA and ASIC
- Silicon and FPGA proven
- Easy SoC integration
- Full implementation and maintenance support with individual approach
- Flexible licensing scheme

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CC-APB_RTC Generic Parameters

Generic name	Description	Type	Range
RTC_width	RTC timer counter width	integer	1:32
prescaler_width	Prescaler counter width	integer	1:32
debounce_counter_width	Debounce counter width	integer	1:32
default_interrupt_MAPPING	Reset value of interrupt_MAPPING register	integer	1:32767

CC-LP_RTC Generic Parameters

Generic name	Description	Type	Range
RTC_width	RTC timer counter width	integer	1:32
prescaler_width	Prescaler counter width	integer	1:32
debounce_counter_width	Debounce counter width	integer	1:32

CC-LP_RTC Pin-out Description

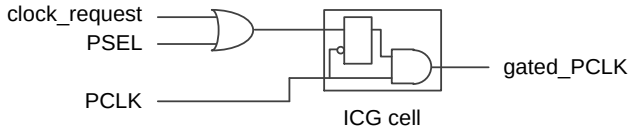
Pin name	Description	I/O	Active
LP_nRST	Asynchronous low power reset	I	low
LP_CLK	Synchronous low power clock	I	rising
PRESETn	Asynchronous host reset	I	low
PCLK	Synchronous host clock	I	rising
HS_DATA_OUTPUT[3:0]	Data output	O	data
HS_DATA_INPUT[3:0]	Data input	I	data
HS_DATA_WRITE	Data write	I	high
HS_DATA_READ	Data read	I	high
HS_RDY	Data ready	I	high
HS_ACK	Data acknowledge	O	high
HS_ERR	Data error	O	high
HS_BUSY	Data busy	O	high
HS_debug_mode	Debug mode input	I	high
LP_OVF_event	Overflow event	O	high
LP_COMPARE_MATCH_event	Campare match event	O	high
LP_WKUP0_event	WKUP0 event	O	high
LP_TIMESTAMP_CAPTURED_event	Timestamp captured event	O	high
LP_WAKE_UP	Host wake-up	O	high
LP_clock_request	Clock request	O	high
WKUP0	WKUP0 input	I	conf.
SHDN	SHDN output	O	conf.
SHDN_oe	SHDN output enable	O	high

CC-APB_RTC Pin-out Description

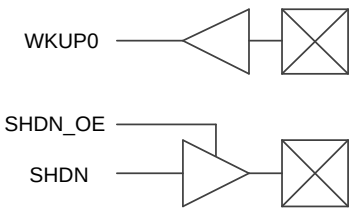
Pin name	Description	I/O	Active
PCLK	Synchronous clock	I	rising
PRESETn	Asynchronous reset	I	low
PSEL	APB peripheral select	I	high
PENABLE	APB bus enable	I	high
PADDR[6:2]	APB bus address	I	data
PWRITE	APB bus write	I	high
PWDATA[31:0]	APB bus write data	I	data
PREADY	APB bus ready	O	high
PRDATA	APB bus read data	O	data
LP_DATA_OUTPUT[3:0]	Data output	O	data
LP_DATA_INPUT[3:0]	Data input	I	data
LP_DATA_WRITE	Data write	O	high
LP_DATA_READ	Data read	O	high
LP_RDY	Data ready	O	high
LP_ACK	Data acknowledge	I	high
LP_ERR	Data error	I	high
LP_BUSY	Data busy	I	high
LP_OV_event	Overflow event	I	high
LP_COMPARE_MATCH_event	Campare match event	I	high
LP_WKUP0_event	WKUP0 event	I	high
LP_TIMESTAMP_CAPTURED_event	Timestamp captured event	I	high
interrupt_OVF	Overflow interrupt	O	high
interrupt_COMPARE_MATCH	Compare match interrupt	O	high
interrupt_WKUP0	WKUP0 interrupt	O	high
interrupt_READY	Ready interrupt	O	high
interrupt_TRANSMISSION_ERROR	Transmission error interrupt	O	high
interrupt_TIMESTAMP_CAPTURED	Timestamp captured interrupt	O	high
interrupt_MAPPING[15:1]	Interrupt mappin vactor	O	data
clock_request	Clock request	O	high

Integration example

- Using clock_request pin for low power mode:



- Pad connection example:



Block Diagram