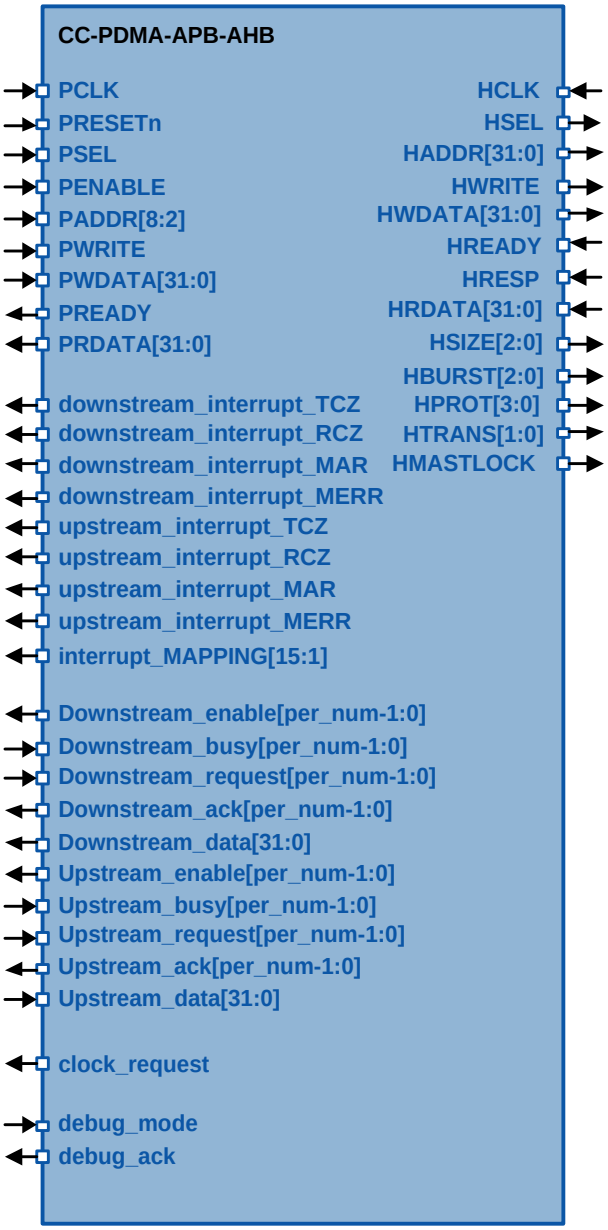
CC-PDMA-APB-AHB Peripheral Direct Memory Access Controller

Symbol



Features

- AMBA APB3 slave bus
- AMBA AHB-Lite master bus
- Configurable number of peripheral channels
- 8, 16, 32 bits data transfer modes
- Upstream and downstream data aggregation to 32 bit chunks
- Various address modes
- Various arbiter priority schemes
- Circular buffer support
- Configurable independent upstream and downstream FIFOs
- Maskable interrupts
- Dedicated upstream and downstream peripherals DMA interface
- Fully synthesizable synchronous design with positive edge clocking
- DFT ready

Benefits

- Supplied as human-readable Verilog RTL source code
- Technology independent IP Core
- Suitable for FPGA and ASIC
- Silicon and FPGA proven
- Easy SoC integration
- Full implementation and maintenance support with individual approach
- Flexible licensing scheme

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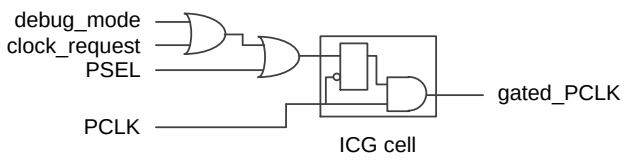
Generic Parameters

Generic name	Description	Type	Range
reg_ADDR_width	APB PADDR signal width	integer	1:32
peripherals_numer	Configure number of peripherals	integer	1:32
peripheral_select _width	Width of the peripheral select register	integer	1:5
downstream_channel _number	Number of downstream channels	integer	1:32
downstream_channel _number_width	Downstream channels number width	integer	1:5
upstream_channel _number	Number of upstream channels	integer	1:32
upstream_channel _number_width	Upstream channels number width	integer	1:5
downstream_data _aggregation _and_FIFO_enable	Enable downstream data aggregation	integer	0, 1
downstream_fifo _depth	Downstream FIFO depth	integer	0:32
downstream_fifo _depth_width	Downstream FIFO depth width	integer	0:5
upstream_data _aggregarion_enable	Enable upstream data aggregation	integer	0, 1
upstream_fifo _depth	Upstream FIFO depth	integer	0:32
upstream_fifo _depth_width	Upstream FIFO depth width	integer	0:5
upstream_fifo_water _level	Water level of upstream FIFO	integer	0:32
default_interrupt _MAPPING	Reset value of interrupt_MAPPING register	integer	0:32767
LOAD_DELAY	Additional register DMA channel output data	integer	0, 1
AHB_HPROT	The value passed to the AHB HPROT output	integer	0:15
BIG_ENDIAN	Endianness of AHB-Lite port	integer	0, 1

Integration example

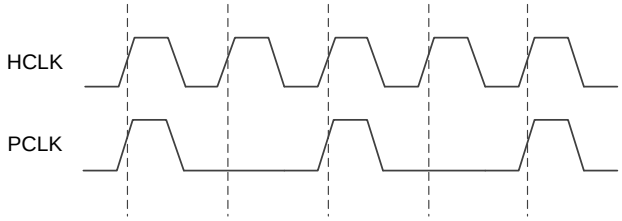
- Using clock_request pin for low power mode:



Pin-out Description

Pin name	Description	I/O	Active
Global signals			
PCLK	Synchronous APB clock	I	rising
PRESETn	Asynchronous reset	I	low
AMBA APB slave signals			
PSEL	APB peripheral select	I	high
PENABLE	APB bus enable	I	high
PADDR [reg_ADDR_width+1:2]	APB bus address	I	data
PWRITE	APB bus write	I	high
PWDATA[31:0]	APB bus write data	I	data
PREADY	APB bus ready	O	high
PRDATA[31:0]	APB bus read data	O	data
Interrupt signals			
downstream _interrupt_TCZ	Transfer counter zero interrupt	O	high
downstream interrupt_RCZ	Reload counter zero interrupt	O	high
downstream interrupt_MAR	Memory address reloaded interrupt	O	high
downstream interrupt_MERR	Memory access error interrupt	O	high
upstream _interrupt_TCZ	Transfer counter zero interrupt	O	high
upstream interrupt_RCZ	Reload counter zero interrupt	O	high
upstream interrupt_MAR	Memory address reloaded interrupt	O	high
upstream interrupt_MERR	Memory access error interrupt	O	high
interrupt_MAPPING[15:1]	Interrupt mapping vector	O	data
Downstream_enable [peripherals_numer-1:0]	PDMA downstream enable signal	O	high
PDMA signals			
Downstream_busy [peripherals_numer-1:0]	PDMA downstream busy signal	I	high
Downstram_request [peripherals_numer-1:0]	PDMA downstream request signal	I	high
Downstream_ack [peripherals_numer-1:0]	PDMA downstream acknowledge signal	O	high
Downstream_data[31:0]	PDMA downstream data	O	data
Upstream_enable [peripherals_numer-1:0]	PDMA upstream enable signal	O	high
Upstream_busy [peripherals_numer-1:0]	PDMA upstream busy signal	I	high
Upstram_request [peripherals_numer-1:0]	PDMA uptream request signal	I	high
Upstream_ack [peripherals_numer-1:0]	PDMA upstream acknowledge signal	O	high
Upstream_data[31:0]	PDMA upstream data	I	data
Debug and power management signals			
clock_request	Clock request signal	O	high
debug_mode	Debug mode input	I	high
debug_ack	Debug mode acknowledge	O	high

- Using different clock ratio for AMBA AHB and APB buses:



AMBA AHB-lite master signals			
HCLK	Synchronous AHB clock	I	rising
HSEL	AHB peripheral select	O	high
HADDR[31:0]	AHB bus address	O	data
HWRITE	AHB bus write	O	high
HWDATA[31:0]	AHB bus write data	O	data
HREADY	AHB bus ready	I	high
HRESP	AHB bus response	I	data
HRDATA[31:0]	AHB bus read data	I	data
HSIZE[2:0]	AHB bus transfer size	O	data
HBURST[2:0]	AHB bus transfer burst	O	data
HPROT[3:0]	AHB bus transfer protection control	O	data
HTRANS[1:0]	AHB bus transfer type	O	data
HMASTLOCK	AHB bus locked transfer	O	high

Block Diagram