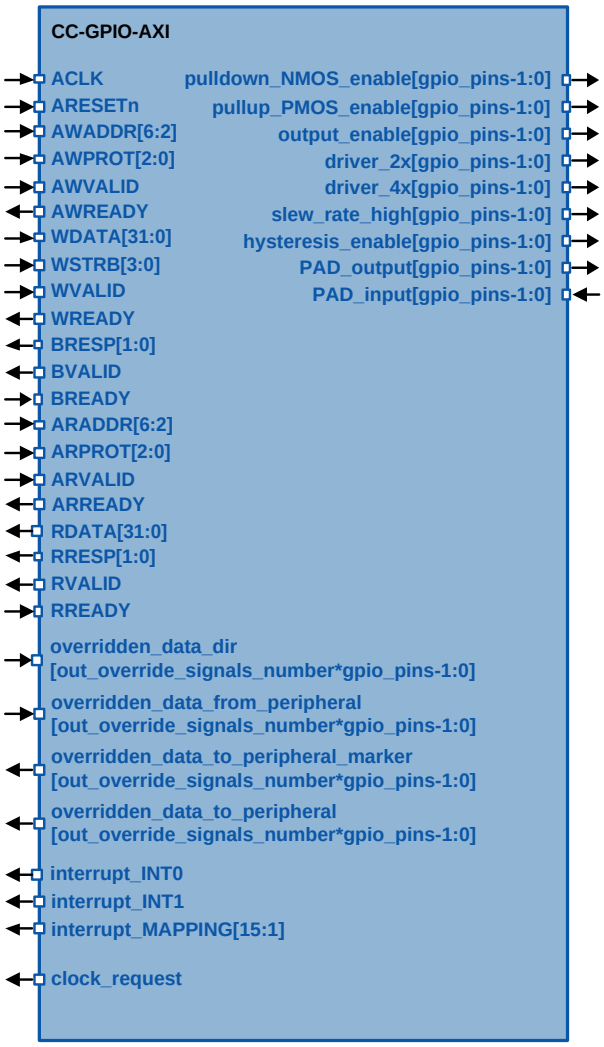
CC-GPIO-AXI General Purpose Input/Output Controller

Symbol



Features

- AMBA AXI4-Lite bus
- Individual configuration of each GPIO pin
- Dynamic programming of each GPIO pin as input or output
- Configurable level or edge triggered interrupts
- Alternative functions support
- Fully synthesizable synchronous design with positive edge clocking
- DFT ready

Benefits

- Supplied as human-readable Verilog RTL source code
- Technology independent IP Core
- Suitable for FPGA and ASIC
- Silicon and FPGA proven
- Easy SoC integration
- Full implementation and maintenance support with individual approach
- Flexible licensing scheme

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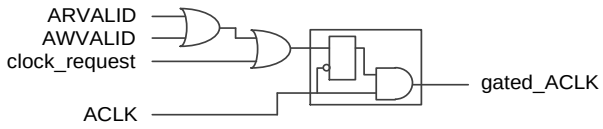
Generic Parameters

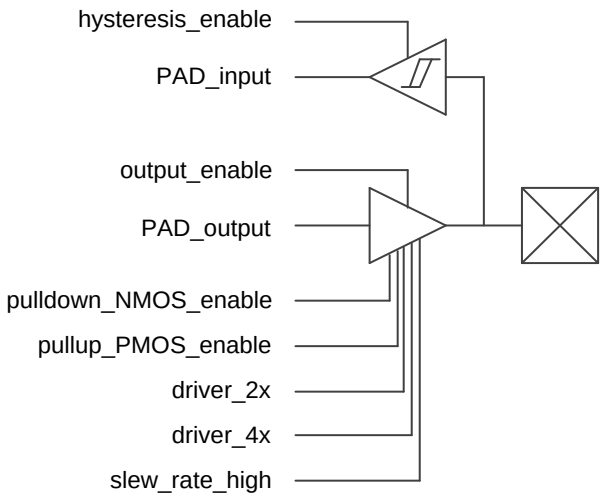
Generic name	Description	Type	Range
gpio_pins	Number of GPIO pins	integer	1:32
out_override _signals_number	Number of GPIO alternative functions	integer	0, 1, 3
out_override _select_width	Width of alternative functions select register	integer	0, 1, 2
default_interrupt _MAPPING	Reset value of interrupt_MAPPING register	integer	0:32767

Integration example

- Using clock_request pin for low power mode:



- Pad connection example:



Pin-out Description

Pin name	Description	I/O	Active
ACLK	Synchronous clock	I	rising
ARESETn	Asynchronous reset	I	low
AWADDR[5:2]	AXI write address	I	data
AWPROT[2:0]	AXI write address protection type	I	data
AWVALID	AXI write address valid	I	high
AWREADY	AXI write address ready	O	high
WDATA[31:0]	AXI write data	I	data
WSTRB[3:0]	AXI write strobe	I	high
WVALID	AXI write valid	I	high
WREADY	AXI write ready	O	high
BRESP[1:0]	AXI write response	O	data
BVALID	AXI write response valid	O	high
BREADY	AXI write response ready	I	high
ARADDR[5:2]	AXI read address	I	data
ARPROT[2:0]	AXI read address protection type	I	data
ARVALID	AXI read address valid	I	High
ARREADY	AXI read address ready	O	high
RDATA[31:0]	AXI read data	O	data
RRESP[1:0]	AXI read response	O	data
RVALID	AXI read valid	O	high
RREADY	AXI read ready	I	high
pulldown_NMOS_enable [gpio_pins-1:0]	Pull down enable signal	O	high
pullup_PMOS_enable [gpio_pins-1:0]	Pull up enable signal	O	high
output_enable [gpio_pins-1:0]	Output enable signal	O	high
driver_2x [gpio_pins-1:0]	Driver 2x selection signal	O	high
driver_4x [gpio_pins-1:0]	Driver 4x selection signal	O	high
slew_rate_high [gpio_pins-1:0]	High slew rate enable signal	O	high
hysteresis_enable [gpio_pins-1:0]	Hystereris enable signal	O	high
PAD_output [gpio_pins-1:0]	Driver output signal	O	data
PAD_input [gpio_pins-1:0]	Pad input signal	I	data
overridden_data_dir [out_override_signals_number *gpio_pins-1 : 0]	Alternative functions direction signal	I	high
overridden_data _from_peripheral [out_override_signals_number *gpio_pins-1 : 0]	Alternative functions data from peripherals	I	data
overridden_data _to_peripheral_marker [out_override_signals_number *gpio_pins-1 : 0]	Alternative functions selection marker	O	high
overridden_data _to_peripheral [gpio_pins-1:0]	Alternative functions data to peripherals	O	data
interrupt_INT0	INT0 interrupt line	O	high
interrupt_INT1	INT1 interrupt line	O	high
interrupt_MAPPING[15:1]	Interrupt mapping vector	O	data
clock_request	Clock request signal	O	high

Internal GPIO pin structure