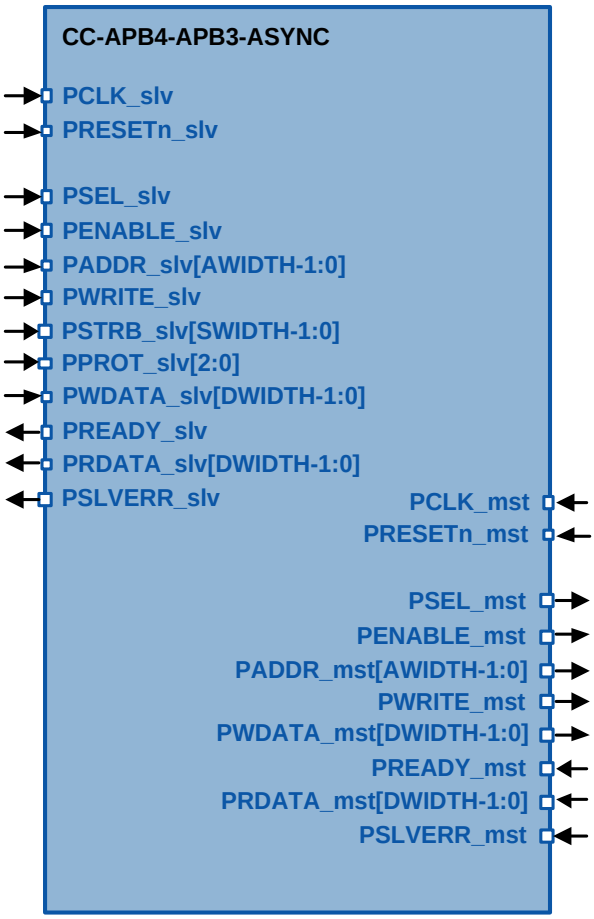
CC-APB4-APB3-ASYNC Asynchronous APB4 to AP3 Bridge

Symbol



Features

- AMBA APB4 Slave
- AMBA APB3 Master
- Supports asynchronous clock ratio
- Transparent addressing
- Issues slave error on non full word write access
- Fully synthesizable design with two positive edge clocking clock domains
- DFT ready

Benefits

- Supplied as human-readable Verilog RTL source code
- Technology independent IP Core
- Suitable for FPGA and ASIC
- Easy SoC integration
- Full implementation and maintenance support with individual approach
- Flexible licensing scheme

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Generic Parameters

Generic name	Description	Type	Range
AWIDTH	Address width	integer	1:32
DWIDTH	Data width	integer	1:32
SWIDTH	Strobe width	integer	1:32

Pin-out Description

Pin name	Description	I/O	Active
PCLK_slv	Synchronous slave clock	I	rising
PRESETn_slv	Asynchronous slave reset	I	low
PSEL_slv	APB4 slave peripheral select	I	high
PENABLE_slv	APB4 slave bus enable	I	high
PADDR_slv [AWIDTH-1:0]	APB4 slave bus address	I	data
PWRITE_slv	APB4 slave bus write	I	high
PSTRB_slv [SWIDTH-1:0]	APB4 slave bus strobe	I	high
PPROT_slv[2:0]	APB4 slave bus protection	I	data
PWDATA_slv [DWIDTH-1:0]	APB4 slave bus write data	I	data
PREADY_slv	APB4 slave bus ready	O	high
PRDATA_slv [DWIDTH-1:0]	APB4 slave bus read data	O	data
PSLVERR_slv	APB4 slave bus error	O	high
PCLK_mst	Synchronous master clock	I	rising
PRESETn_mst	Asynchronous master reset	I	low
PSEL_mst	APB3 master peripheral select	O	high
PENABLE_ mst	APB3 master bus enable	O	high
PADDR_ mst [AWIDTH-1:0]	APB3 master bus address	O	data
PWRITE_ mst	APB3 master bus write	O	high
PWDATA_ mst [DWIDTH-1:0]	APB3 master bus write data	O	data
PREADY_ mst	APB3 master bus ready	I	data
PRDATA_ mst [DWIDTH-1:0]	APB3 master bus read data	I	data
PSLVERR_ mst	APB3 master bus error	I	high