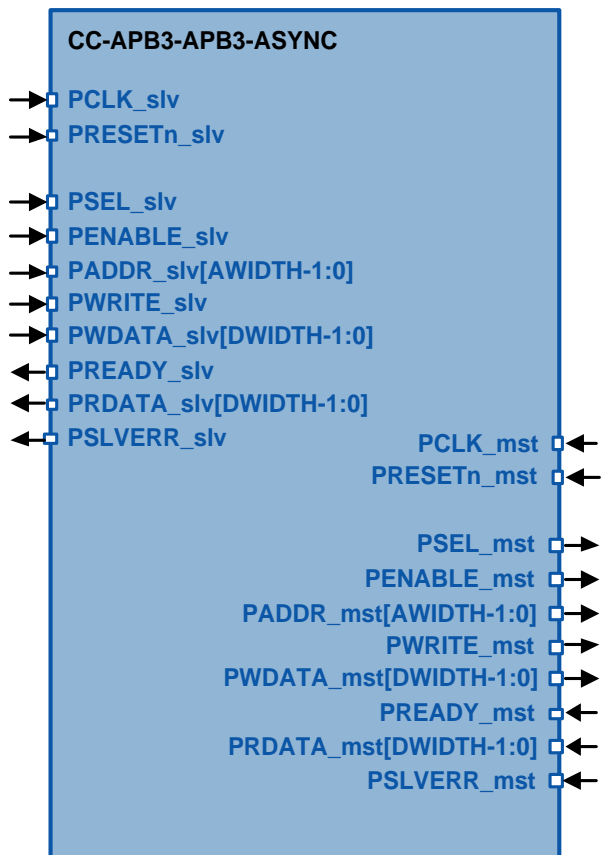


## CC-APB3-APB3-ASYNC Asynchronous APB3 to AP3 Bridge

### Symbol



### Features

- AMBA APB3 Master
- AMBA APB3 Slave
- Supports asynchronous clock ratio
- Transparent addressing
- Fully synthesizable design with two positive edge clocking clock domains
- DFT ready

### Benefits

- Supplied as human-readable Verilog RTL source code
- Technology independent IP Core
- Suitable for FPGA and ASIC
- Easy SoC integration
- Full implementation and maintenance support with individual approach
- Flexible licensing scheme

## Generic Parameters

Generic name	Description	Type	Range
AWIDTH	Address width	integer	1:32
DWIDTH	Data width	integer	1:32

## Pin-out Description

Pin name	Description	I/O	Active
PCLK_slv	Synchronous slave clock	I	rising
PRESETn_slv	Asynchronous slave reset	I	low
PSEL_slv	APB slave peripheral select	I	high
PENABLE_slv	APB slave bus enable	I	high
PADDR_slv [AWIDTH-1:0]	APB slave bus address	I	data
PWRITE_slv	APB slave bus write	I	high
PWDATA_slv [DWIDTH-1:0]	APB slave bus write data	I	data
PREADY_slv	APB slave bus ready	O	high
PRDATA_slv [DWIDTH-1:0]	APB slave bus read data	O	data
PSLVERR_slv	APB slave bus error	O	high
PCLK_mst	Synchronous master clock	I	rising
PRESETn_mst	Asynchronous master reset	I	low
PSEL_mst	APB master peripheral select	O	high
PENABLE_mst	APB master bus enable	O	high
PADDR_mst [AWIDTH-1:0]	APB master bus address	O	data
PWRITE_mst	APB master bus write	O	high
PWDATA_mst [DWIDTH-1:0]	APB master bus write data	O	data
PREADY_mst	APB master bus ready	I	data
PRDATA_mst [DWIDTH-1:0]	APB master bus read data	I	data
PSLVERR_mst	APB master bus error	I	high

