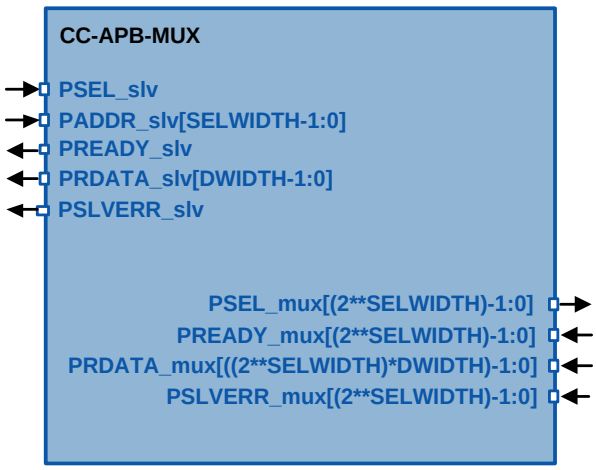
CC-APB-MUX Peripheral APB Multiplexer

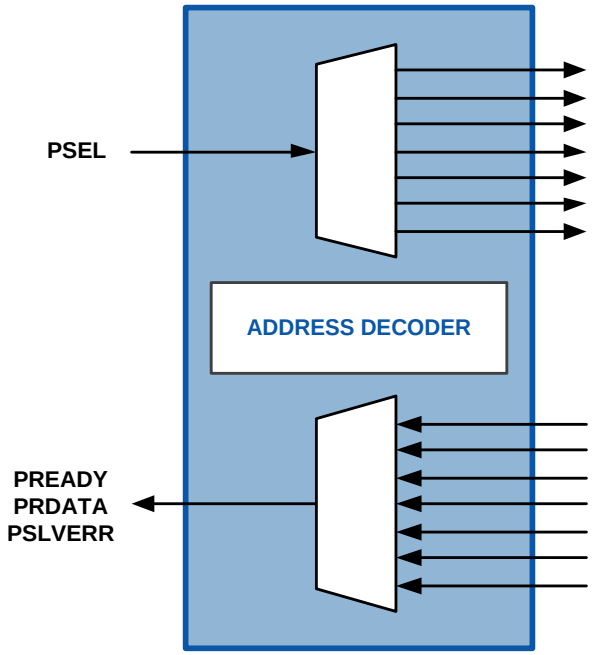
Symbol



Features

- AMBA APB3 bus multiplexer
- Flexible peripheral number
- Flexible addressing partitioning through multiplexer stacking
- Fully combinational design
- DFT ready

Block diagram



Benefits

- Supplied as human-readable Verilog RTL source code
- Technology independent IP Core
- Suitable for FPGA and ASIC
- Easy SoC integration
- Full implementation and maintenance support with individual approach
- Flexible licensing scheme

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Generic Parameters

Generic name	Description	Type	Range
ADDRWIDTH	Address width	integer	1:32
SELWIDTH	Address selection width	integer	1:32
DWIDTH	Data width	integer	1:32

Pin-out Description

Pin name	Description	I/O	Active
PSEL_slv	APB slave peripheral select	I	high
PADDR_slv [ADDRWIDTH-1:0]	APB slave bus address selection	I	data
PREADY_slv	APB slave bus ready	O	high
PRDATA_slv [DWIDTH-1:0]	APB slave bus read data	O	data
PSLVERR_slv	APB slave bus error	O	high
PSEL_mux [(2**SELWIDTH)-1:0]	APB multiplexer PSEL	O	high
PREADY_mux [(2**SELWIDTH)-1:0]	APB multiplexer PREADY	I	high
PRDATA_mux [((2**SELWIDTH)*DWIDTH)-1:0]	APB multiplexer PRDATA	I	data
PSLVERR_mux [(2**SELWIDTH)-1:0]	APB multiplexer PSLVERR	I	high

Multiplexer stacking