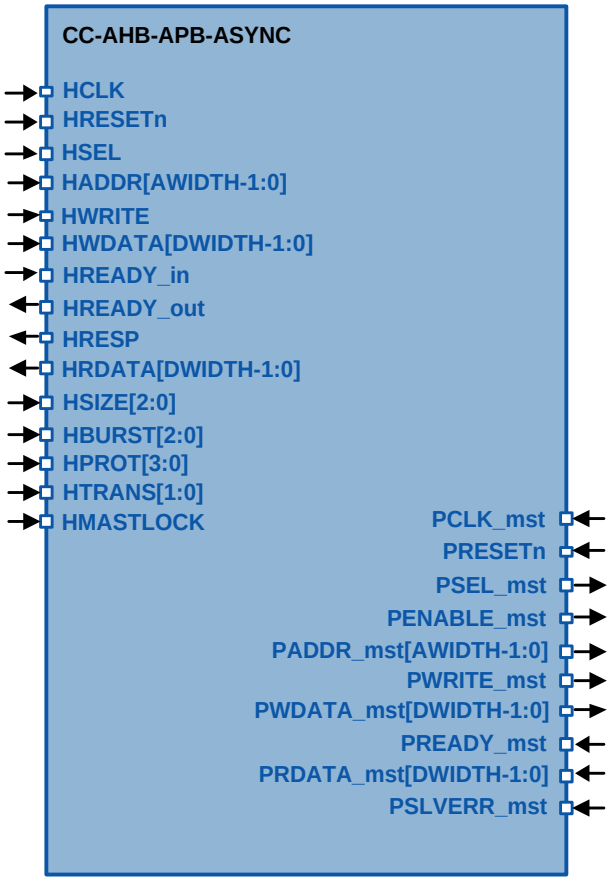
CC-AHB-APB-SYNC Asynchronous AHB to APB Bridge

Symbol



Features

- AMBA AHB Slave
- AMBA APB3 Master
- Supports asynchronous clock ratio
- Transparent addressing
- Fully synthesizable design with two positive edge clocking clock domains
- DFT ready

Benefits

- Supplied as human-readable Verilog RTL source code
- Technology independent IP Core
- Suitable for FPGA and ASIC
- Easy SoC integration
- Full implementation and maintenance support with individual approach
- Flexible licensing scheme

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Generic Parameters

Generic name	Description	Type	Range
AWIDTH	Address width	integer	1:32
DWIDTH	Data width	integer	1:32

Pin-out Description

Pin name	Description	I/O	Active
HCLK	Synchronous AHB clock	I	rising
HRESETn	Asynchronous AHB reset	I	low
HSEL	AHB peripheral select	I	high
HADDR[AWIDTH-1:0]	AHB bus address	I	data
HWRITE	AHB bus write	I	high
HWDATA[DWIDTH-1:0]	AHB bus write data	I	data
HREADY_in	AHB bus ready input	I	high
HREADY_out	AHB bus ready output	O	high
HRESP	AHB bus response	O	data
HRDATA[DWIDTH-1:0]	AHB bus read data	O	data
HSIZE[2:0]	AHB bus transfer size	I	data
HBURST[2:0]	AHB bus transfer burst	I	data
HPROT[3:0]	AHB bus transfer protection control	I	data
HTRANS[1:0]	AHB bus transfer type	I	data
HMASTLOCK	AHB bus locked transfer	I	high
PCLK	Synchronous APB clock	I	rising
PRESETn	Asynchronous APB reset	I	low
PSEL_mst	APB master peripheral select	O	high
PENABLE_ mst	APB master bus enable	O	high
PADDR_ mst [AWIDTH-1:0]	APB master bus address	O	data
PWRITE_ mst	APB master bus write	O	high
PWDATA_ mst [DWIDTH-1:0]	APB master bus write data	O	data
PREADY_ mst	APB master bus ready	I	data
PRDATA_ mst [DWIDTH-1:0]	APB master bus read data	I	data
PSLVERR_ mst	APB master bus error	I	high