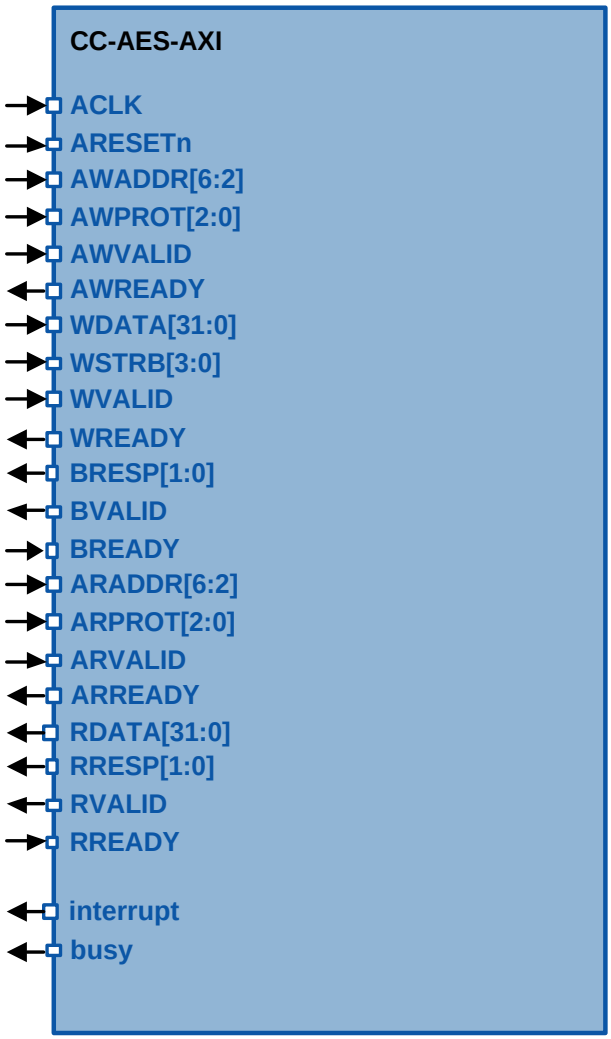
CC-AES-AXI Advanced Encryption Standard Core

Symbol



Features

- AMBA AXI4-Lite bus
- Encryption and/or decryption
- ECB mode
- 128 bit data block
- Programmable 128, 192, 256 bit key length
- Fully synthesizable synchronous design with positive edge clocking
- DFT ready

Benefits

- Supplied as human-readable Verilog RTL source code
- Technology independent IP Core
- Suitable for FPGA and ASIC
- Silicon and FPGA proven
- Easy SoC integration
- Full implementation and maintenance support with individual approach
- Flexible licensing scheme

Throughput (including interface)

Key length	Throughput
128-bit	2.61 bits/cycle
192-bit	2.51 bits/cycle
256-bit	2.42 bits/cycle

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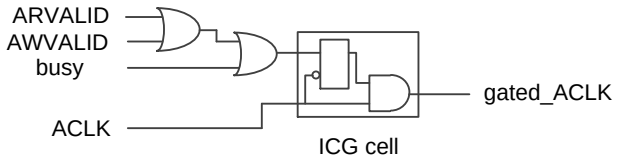
Generic Parameters

Generic name	Description	Type	Range
DECRYPTION_PATH	Configure AES core decryption support	integer	0, 1

Integration example

- Using clock_request pin for low power mode:



Pin-out Description

Pin name	Description	I/O	Active
ACLK	Synchronous clock	I	rising
ARESETn	Asynchronous reset	I	low
AWADDR[6:2]	AXI write address	I	data
AWPROT[2:0]	AXI write address protection type	I	data
AWVALID	AXI write address valid	I	high
AWREADY	AXI write address ready	O	high
WDATA[31:0]	AXI write data	I	data
WSTRB[3:0]	AXI write strobe	I	high
WVALID	AXI write valid	I	high
WREADY	AXI write ready	O	high
BRESP[1:0]	AXI write response	O	data
BVALID	AXI write response valid	O	high
BREADY	AXI write response ready	I	high
ARADDR[6:2]	AXI read address	I	data
ARPROT[2:0]	AXI read address protection type	I	data
ARVALID	AXI read address valid	I	High
ARREADY	AXI read address ready	O	high
RDATA[31:0]	AXI read data	O	data
RRESP[1:0]	AXI read response	O	data
RVALID	AXI read valid	O	high
RREADY	AXI read ready	I	high
interrupt	AES interrupt	O	high
busy	AES busy	O	high